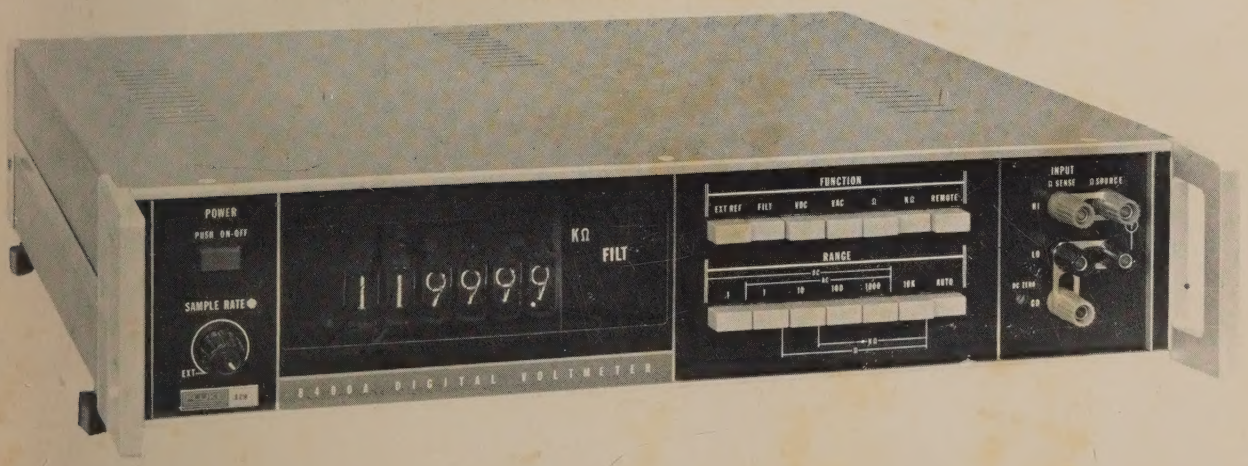
model 8400

DIGITAL VOLTMETER



FLUKE®

STUDENT HANDOUT

Introduction

This training course has been prepared by the Customer Service Department of the John Fluke Mfg. Co., Inc. to assist the experienced technician to understand how the instrument works, how to calibrate it and how to maintain it. This manual is intended as a supplement to the Audio/Visual training package of the same title. It is suggested that prior to attending this course of instruction, the course titled "Recirculating Remainder" should have been completed. Should you have any questions, comments or suggestions about this course of instruction please feel free to communicate them to the Training Department by letter or telephone.

Customer Service Training Dept.

John Fluke Mfg. Co., Inc.

P.O Box 7428 • Seattle, Washington 98133

Tel: (206) 774-2409

Litho in U.S.A. 1-73

INTRODUCTION

The Model 8400A Digital Voltmeter is a five decade instrument with 20% over-ranging. Its main frame accepts a variety of analog and systems options that may be installed in the field at any time and in any sequence making it possible at any time to convert the instrument into a full system multimeter. Options include the AC Converter –01 Option, Resistance Converter –02 Option, Data Output Unit –03 Option, Remote Controlled Unit –04 Option, DC External Reference –05 Option, and AC External Reference –06 Option.

The 8400A uses the Recirculating Remainder analog to digital conversion technique which periodically samples the input and serially digitizes the sample providing a reliable DVM with a high long term accuracy and linearity, and outstanding environmental characteristics coupled with long term reliability.

BASIC 8400A

The basic 8400A measures DC voltages in five ranges with up to 1 microvolt of resolution and 20% over-ranging with an 1100 volt overload capacity. A non-blinking read-out contains an in line neon tube display showing polarity, over-range digit, and five full decades of digits. The speed at which the read-out updates, i.e. the input is sampled, is controllable by a variable Sample Rate Control available in both front panel adjustment and remote control operation. A switchable four pole filter has true broad band noise rejection that cannot integrate a constant offset error into the reading. The filter may be used with all analog options.

ANALOG OPTIONS

The AC Converter –01 Option makes it possible for the 8400A to measure AC voltages from 10 Hz to 100 kHz with up to 10 μV of resolution with a voltage limit of 1100 volts. A zero control is not needed to maintain the extremely low percent of range proportions of the specifications. The Resistance Converter –02 Option provides the instrument with seven resistance ranges from 10Ω to 10,000 KΩ making it possible to measure resistance up to 12 megohms. With the –02 resistance option installed, true four terminal measurements through the 10,000 KΩ range may be made. The DC External Reference Option provides four terminal DC to DC ratio measurements with ranges of $\pm$.01:1 to $\pm$100:1 while the AC External Reference Option provides three terminal AC to AC ratio measurements with reference ranges from 1 volt to 100 volts. Systems options such as the Isolated Remote Control and Isolated Data Output provide the instrument with complete systems interface capability.

BLOCK DIAGRAMS

BUFFER (A11) Figure No. 2

The Buffer, as shown in Block Diagram Figure 3, consists of an Input Divider which serves to attenuate the input. An Amplifier with a switchable gain for millivolt measurements followed by an Inverting Amplifier. It also contains the Logic circuitry required for Auto Ranging functions in the DC volts mode of operation.

The output voltage of the Buffer is zero to $\pm$10 volts inverted.

ACTIVE FILTER (A10) Figure No. 4

The Active Filter suppresses AC noise present in the Buffer output. It consists of a Voltage Follower and a Four Pole Filter. The filter may be selected by front panel or remote control. When filtering is not selected the circuit functions as a unity gain voltage follower. The output of the Active Filter is fed to the A-to-D Converter Assembly.

A-TO-D CONVERTER (A9) Figure No. 5

The A-to-D Converter consists of an Inverting Amplifier followed by a Polarity Detector and Switching system which feeds the A-to-D Amplifier. Display Storage, Sample and Hold, the Analog Comparator, the Ladders, and the Inverting Amplifier and Auto Zero Drive circuits are all located on this assembly.

The A-to-D Converter receives output from the Active Filter, detects the polarity, and switches the input FET's in such a manner as to always apply the input voltage to the amplifier in such a manner that its output is always positive. The output of the A-to-D Amplifier is connected to an Analog Comparator. The Analog Comparator produces current whenever the voltage out of the A-to-D Amplifier is above a predetermined level. It supplies its output current to the Constant Current Oscillator in the Logic Assembly.

Sample and Hold storage is included in the A-to-D Converter Assembly. Remainders of each digitizing period are stored alternately on the capacitors in Sample and Hold. When the instrument is in the Measurement Mode of operation, Display Storage stores analog values of digitized quantities in five separate capacitors. Display Storage consists of seven FET's connected in such a manner as to store these analog increments. Ladder Drivers cause the incremental switching in the Primary and Secondary Ladder circuits. The Primary Ladder feeds back to the input of the A-to-D Amplifier and the Secondary Ladder feeds the Display Storage through a monolithic amplifier.

LOGIC (A8) Figure No. 6

The Logic Control circuitry contains the Master Clock which produces 666 pulses per second which is coupled to a Six State Shift Register which generates the basic digitizing time periods. The Logic Assembly also contains the Current Controlled Oscillator which feeds the 16 State Binary Counter which translates the output of the Current Controlled Oscillator into BCD format. The Ladder Switches are also contained in the Logic Assembly.

Display Storage control pulses and the Analog Cycle Control pulses are generated in the Logic Assembly. These pulses control the various functions of the analog to digital conversion technique. The +7 Volts Reference Supply is also located on the Logic Assembly.

DISPLAY ASSEMBLY (A14) Figure No. 7

In addition to the seven gas filled display tubes and the Decoder Driver, the Display Assembly also contains the Anode Strobing circuitry used to display the digitized numbers in sequence as they are developed. Polarity Memory and Function Display are also contained in this assembly. The Sample Command Oscillator which controls the Measure and Storage time relationship is contained on this board, as is the Range Counter circuitry which provides the autoranging function throughout the instrument. Range and Function switches are also mounted on this assembly.

RANGE DELAY (A2) Figure No. 8

The Range Delay processes switching inputs from the front panel and produces control commands for the Range Decoder in the Display Assembly. It also produces UP and DOWN Autorange

commands for the Range Counter. The circuit consists of Logic, Range Delay 1 Shot, and a Pulse Generator. The Logic circuitry produces control signals for the Pulse Generator and the Decoder in the A14 Display Assembly. A clock signal for the Range Counter in the A14 Display is produced by the Pulse Generator. This clock signal is required for the Auto-range feature. The Range Delay 1 Shot produces a program time delay after any range change to allow for settling time of the analog signal conditioners which process the input.

POWER SUPPLY (A1) Figure No. 2

Four separate, but interdependent power supplies are contained in this assembly. A 200 volt Anode supply, +18 and −18 Operating supplies and a +5 volt Logic supply. The +5 volts is regulated by a reference voltage drop from the −18 volt supply.

CIRCUIT DESCRIPTIONS

BUFFER ASSEMBLY (A11) Drawing No. 8400A-1005

The Buffer consists of four basic elements. Input and Output voltage dividers, Amplifiers, and Control logic. The circuit has two operating configurations or modes as determined by the voltage selected, a low volts mode and a high volts mode. In the low volts mode, the 0.1 and 1.0 volt range, amplification of the input is required. In the high voltage modes, 100 and 1,000 volt ranges input attenuation occurs. In the 10 volt range, the input is processed without attenuation or amplification, since the output of the Buffer is zero to ±10 volts. The low volt input is applied across current limiting resistor R2, through the contacts of K1 to the high input impedance amplifier composed of three separate amplifiers - - a dual differential, operational amplifier composed of Q4 and Q5, U1, and an inverting amplifier U2. The output of the amplifier is applied in parallel to the A10 Active Filter and to a gain determining output voltage divider R37 through R40, through contacts of relays K1 and K6. In the low volt mode of operation voltage follower U3 is used to boot strap the operational environment of the input dual differential pair Q4 and Q5 with the input voltage to increase its effective ratio of common mode rejection. Offset voltage present that would cause Buffer output with no input, is compensated for by use of two potentiometers, one a coarse DC ZERO which balances the basic meter voltages of the input to the differential amplifier Q5 by adjusting the collector current ratio; and the second potentiometer Buffer ZERO which affords a fine adjustment, by applying just that amount of known voltage to the base of differential amplifier Q5B, that results in a Buffer output voltage equal to zero when the input voltage is zero. Buffer ZERO, which is the fine adjustment, is available via a front panel access.

Overload protection for the dual differential amplifier is afforded by CR1, R2, Q11, and the current limiting resistors previously defined as R1 and R2 shown on the wiring diagram. Positive overload protection is afforded by transister Q11 which clamps the amplifier output to 1.7 volts. Negative over-voltage protection is afforded by diode CR1 which clamps the input to −1.7 volts. The current drawn during an overload is limited by the total input resistance of 147 K ohms.

Compensation circuits have been provided to reduce the temperature coefficient of the input offset voltage and offset current. Transistor Q2 and the surrounding circuitry, R18 and R19, provides the temperature variable base current required by input transistor Q5. Transistor Q3 compensates the temperature variation of the basic meter voltage in dual transistor Q4 to insure that the input transistor Q5 remains at substantially the same bias condition, irrespective of temperature.

ACTIVE FILTER (A10) Drawing No. 8400A-1015

The Active Filter as shown in schematic drawing number 8400A-1015 consists of a voltage follower proceeded by four poles of low pass filtering. These poles attenuate undesirable AC signals which

may be present on the DC input signal. Filtering occurs after the FILT switch has been depressed or filtering called for by the remote controlled unit when the instrument is in a systems application. A block diagram of the active filter is shown in Figure 4. An Active Filter is used for better response time.

A-to-D CONVERTER (A9) Drawing No. 8400A-1003

Inverting Amplifier

Input from the Active Filter is fed to the Inverting Amplifier whose output is connected to the Polarity Detector and to the minus input to the A-to-D Amplifier. The Polarity Detector detects the polarity and switches Q7 or Q8 in such a fashion as to always place a positive voltage on the input of Q20. When the input is positive, FET Q8 turns ON and applies a positive input to transistor Q20. Conversely, when the input to the instrument is negative, Q10 senses the negative voltage and switches Q7 which takes the positive output out of the Inverting Amplifier and applies the positive output to the input of Q20. Thus, input to the A-to-D Amplifier is always positive on the "A" side of Q20. An Automatic ZERO drive circuit consisting of transistors Q5, Q6, and capacitor C2 has been included. The Auto ZERO signal also drives transistor Q3 to turn OFF, thereby removing input to the Inverting Amplifier during the ZERO Offset correction time period. The GATE 4 signal is applied to the emitters of Q10 and Q11 in the Polarity Detector, enabling the Polarity Detector only during the "A" digitizing period when the instrument is in Measurement Mode. During the remainder of measurement period the plus and minus gates Q7 and Q8 are turned OFF and polarity information is retained by the display circuit, Polarity Memory.

A-to-D Amplifier

The A-to-D Amplifier consists of dual FET Q20 and monolithic amplifier U2 and the associated components. The offset removal circuit is composed of transistors Q23, Q24, and capacitor C7. Switch Q24 is turned ON during the ZERO time period when the instrument is in Measurement Mode. This signal also controls switches Q19 and Q31 which are turned ON during the ZERO time period. Q30 which is turned OFF during the ZERO time period to disconnect the Amplifier output from the Ladder. Transistor Q29 and resistor R54 constitute a clamp which prevents the A-to-D Amplifier from saturating when its output is above 7 volts.

Analog Comparator (A9)

The Analog Comparator consisting of Q32, Q33, Q34, and Q35 is a voltage comparator. Differential amplifier Q35 compares the A-to-D Amplifier output with a +7 reference and Q33, Q34 outputs the resultant current to the Current Control Oscillator. Transistor Q32 operates as a second comparator which responds quickly to high voltage levels, thereby allowing maximum time for the resolution of the last pulse.

The Sample and Hold circuit consists of transistors Q25 through Q28, and capacitors C9 and C10. The sequence of operation is as follows: C9 stores the first remainder, C10 stores the second remainder, C9 the third remainder, C10 the fourth remainder, C9 the fifth remainder. The remainders are alternately stored and released by the action of the FET switches Q25 through Q28 and the gate pulses GATE 2, GATE 1-22 and GATE 11.

Ladders

The Ladders are controlled by the Ladder Switches Q37 through Q44 which are driven by the Ladder Drivers located on the Logic Assembly (A8). The output of the Ladder Switches is

applied to two Ladders simultaneously. Each Ladder comprises a four-bit weight resistor digital to analog converter. The Primary Ladder consists of resistors R44 through R50 and produces an output that corresponds to the actual value of the digital input. The Secondary Ladder which drives only the display storage circuits through Buffer Amplifier U3, consists of resistors R40 through R43 and produces an analog value that is proportional to the digit that has been digitized in each period. A half digit bias is produced by R38 and R39 in conjunction with the Secondary Ladder's resistors and adds the voltage equivalent of half a digit to the output of the Secondary Ladder. This insures proper display storage by compensating for the effects of any possible voltage decay in the storage circuit.

Display Storage

The Display Storage circuit consists of FET switches Q13 through Q37, capacitors C11 through C15, and FET switches Q12 and Q18. The buffered output of the Secondary Ladder is supplied to the appropriate storage capacitor through Q18, which is enabled during the second half of each digitizing period. The first and most significant digit is stored on C13 and the least significant digit is stored as a charge on C14. These capacitors receive their analog charge in Measurement Mode as each digit is initially digitized. Q12, the output FET, is not enabled until Storage Mode and then places the output of each capacitor on the input of the A-to-D Amplifier and as each analog value is redigitized, during the last half of each time period, that digit is replaced as an analog charge in its respective capacitor by the action of Q18. Thus, the same reading is continually digitized and displayed until a new sample is taken.

LOGIC (A8) Drawing No. 8400A-1004

The Logic Assembly contains a Master Clock and a Shift Register that generate and divide to produce the timing functions for the instrument. In addition, it contains the Constant Current Oscillator and Binary Counter plus the 7 Volt Reference Supply.

Master Clock

The 333 Hz clock signal is produced by transistor Q1. The clock frequency is determined by the RC time constant of resistor R1 and capacitor C1. The output of the Clock is applied to the clock input of flip-flop U1B. The Q output of U1B is inverted by Q4 and becomes the $\overline{H}$ signal.

Shift Register

The 6 State Shift Register consists of 5 J-K flip-flops U3A, U3B, U4A, and U1A. U2B is used to generate the $\overline{ZERO}$ pulse which is the first timing period of each cycle of the instrument. When the NAND gate U2B receives all high signals from the $\overline{A}$ through $\overline{E}$ lines it produces a $\overline{ZERO}$ pulse. The Q outputs of the Shift Register supply the A through E digitizing period pulses. Outputs from the 6 State Shift Register are also fed to Display Storage Control which generates the storage pulses used in display storage in the A-to-D Converter Assembly.

Constant Current Oscillator

The Constant Current Oscillator consisting of a multivibrator Q1 and Q3 generates a pulse train whenever it is supplied current by the Analog Comparitor. The pulse train is fed to a 16 State Binary Counter. The binary output of that counter is fed to the Ladder Switches and to the Decoder Driver in the Display Assembly. The truth table for the 16 State Binary

Counter is shown in Figure 13. Directly below the 16 State Binary Counter are shown four transistors Q19 through Q22 which are the Ladder Switches and are connected to the Ladder Drivers located on the A-to-D Assembly.

Analog Cycle Control

The Analog Cycle Control consisting of Q11 through Q17 and accepts various basic time pulses and generates the special pulses such as the GATE pulses, STORE IN and STORE OUT pulses.

+7 Volt Reference Supply

The 7 Volt Reference for the instrument is derived by using a Reference Amplifier, U9, which also encompasses a zener diode reference. Amplifier U10 and emitter follower Q25 are connected as an operational amplifier which presents a low source impedance at the reference point. Transistor Q24 disables the 7 Volt Reference in the event the user wishes to employ an external reference when the required options are installed. Transistor Q23 coupled with the zener diode in the Reference Amplifier produce the +7 Volt Reference.

DISPLAY (A14) Drawing No. 8400A-1002, Sht. 1 and Sht. 2

The BCD input from the Counter is coupled to Decoder Driver U4. U4 translates the BCD count into a low signal on the appropriate decimal line to the display tubes. Each display tube is pulsed ON in sequence with its respective digitizing period by the pulse appearing at the bases of Q22 through Q26 which are enabled by the $\overline{F}$ pulse appearing at Q34 which means that the display tube can ionize only during the last half of each of the digitizing periods. A11 through Q18 serve to light the decimal points in the Display Assembly by the action of the signals coupled to their emitters and bases. Polarity Memory circuit receives its information from the Polarity Detector. Once having been pulsed, the flip-flop will turn to the appropriate state so that when the C pulse enables the base of Q9 and Q10, whichever is conducting, it can place a low on the appropriate sign in V1.

Sample Command Oscillator

The Sample Command Oscillator consists of a programmable unijunction transistor, Q8, and the surrounding circuitry. Resistors R12 and R14 provide a bias level for the gate of the Programmable Unijunction Transistor (PUT). C3 charges through R16 and R17 and when the PUT conducts, capacitor C3 is discharged. This generates an output pulse which commands the Measure/Store cycle J-K flip-flop U3A located adjacent to the Range Counter flip-flop. U3A generates the M and $\overline{M}$ pulses which control the Measure time. Varying R16 in the Sample Command Oscillator will vary the sample rate of the instrument. The ZERO pulse fed to the clock input of U3A insures starting the Measure Mode at the beginning of a timing cycle.

If the instrument is ranging, SIGNAL 3 entering the junction of R9 and CR7 in the Sample Command Oscillator will disable Q6 which in turn disables the Sample Command Oscillator to allow time for the analog signal conditioners to settle on the new range before a new Measurement Mode is entered.

When SAMPLE RATE control is switched to the external position and sampling is initiated through the EXTernal trigger, input of the Data Output Unit Option will cause a near ground potential to appear on the emitter of Q6. Its collector follows causing the gate of Q8 to be more than .6 volts below the anode and the Programmable Unijunction Transistor fires once. If the corresponding sample rate results in a range change, the Range Delay One-Shot Multivibrator will disable the Sample Command Oscillator via SIGNAL 3 entering through CR7. This means that Measurement Mode may not be commanded until the Range Delay One-Shot times out. At the end of this time delay the Sample Command Oscillator is automatically retriggered via CR8 and SIGNAL 2 from the Range Delay One-Shot. Diode CR9 and resistor R10 insure that capacitor C3 will rapidly charge to be ready for the next trigger pulse. SIGNAL 8 interrupts the Cycle Control Shift Register on the logic assembly (A8) by forcing it directly to the "E" digitizing period. This is done to minimize the time between the Sample Command to start a Measure Mode and the actual start of that Measure Mode.

Over Range Driver

The Over Range Driver is a means of detecting a maximum count of 12 during the first time period when the instrument is in its highest possible range. This is done through the action of Q3, Q4, and Q5. Q3 has coupled to its base the Constant Current Oscillator output pulses, to its emitter the $\overline{UP}$ pulse. The $\overline{UP}$ occurs on the eleventh count in the "A" time period and goes low enabling transistor Q3. At the next CCO pulse, which would be the twelfth pulse, transistor Q3 will conduct enabling Q5 and placing the 5 volts on DS5 in the function display assembly which will turn on the OVER lamp.

Q4 is a monostable device and requires resetting once it goes into conduction, which is accomplished by the following Measure pulse coupled through C1 which differentiates the signal and resets Q4 turning OFF the OVER lamp. When the Over Range Driver is in its conducting state it produces from the emitter of Q37 a SIGNAL 7 which is used in the Range Delay Assembly to stop the Range Oscillator preventing the instrument from trying to seek a higher range. Q2 located above the Over Range Assembly has no application in the Over Range function. It is used to accept the filter signal which turns on the Input Filter in the instrument causing Q2 to cut off and cause an additional delay in the Range Delay Multivibrator so when filter is selected the Ranging Oscillator is operating at a lower frequency in order to compensate for the additional settling time required in the instrument.

Range Counter

The Range Counter is composed of three J-K flip-flops. Flip-flop U3B has a clocked input that is SIGNAL 6. This signal originates in the Range Oscillator and is pulsed with each firing of the Range Oscillator. The Range Counter is a divide by 6 counter that provides 6 possible binary states for range counting. Five pulses being considered an UP range command and one pulse being considered a DOWN range command. Signal 6 applied to the clock input of the range flip-flop U3B alters the 6 state of the Range Counter. Transistor Q35 is provided to reset U2B which may be in an unallowed state as a result of initial instrument turn ON. The output of U3B is fed back to the clock inputs of U2A and U2B providing their input for a proper Range Code advancement.

RANGE DELAY (A2) Drawing No. 8400A-1006

The Range Delay Assembly consists of Gate, a Range Delay One-Shot Multivibrator, and a Range Oscillator. The gates allow the specified set of ranges to be obtained which is dependent upon the function called. The Range Oscillator generates pulses which trigger the Range Delay One-Shot while simultaneously causing the Range Counter to change states. The Range Delay One-Shot prevents further ranging for a specified time to allow the analog signal conditioners to settle in the new range. This time is variable depending upon whether Filter has been selected or not.

The gates are U2A, U2B, U2C, U3A, and U3B. Gate U2C and U3A are UP range stops. Gate U2C prevents autoranging above the 10,000 range while gate U3A prevents autoranging above the 1,000 range in the VDC function. Gates 2A and 2B are DOWN range stops. Gate U2A prevents autoranging below the 10 range in the ohms function while gate U2B prevents autoranging below 0.1 in any function. Gate U3B is the master UP range control and enables the Range Oscillator only if an UP range is expected.

The three inverters U1D, U1E, and U1F coupled with the UP range enable line provide one input for UP range control gate U3B. The result is that U3B is enabled for 1.5 milliseconds or the second half of the "A" digitizing period of Measurement Mode if an UP range is to be executed.

Signals applied to diodes CR6, CR7, CR8, and CR10 coupled with the range DOWN enable line provide a negative going signal to the range oscillator at the end of the "A" digitizing period in a Measurement Mode if a DOWN range is to be executed.

Range Oscillator

The Range Oscillator is composed of capacitor C4 and resistors R14 and R18 and transistor Q4. The output of this oscillator appears at the cathode of Q4. Q4 is fired discharging capacitor C4 through R15 when the gate is about −.6 volts relative to the anode. Thus, Q4 is fired to produce one output pulse by lowering its gate voltage or by raising its anode voltage such that the voltage difference between these elements is .6 volts. The firing of Q4 discharges capacitor C4 and reduces the anode and gate voltages. Thus, Q3 will turn on and force the anode and gate of Q4 to the same potential. Q4 turns off and capacitor C4 charges through R14 and R15. If the firing potential between the gate and anode of Q4 is established, Q4 fires again and the cycle is repeated to produce the second output pulse. The frequency of oscillations is set by the level of gate voltage applied and the charging time constant of R4, R18, and capacitor C4.

Control of the gate of Q4 is affected by two mutually exclusive inputs. One of these associated with the ranging UP and the other associated with ranging DOWN. In an UP range situation, the output of U3B goes low for about 1.5 milliseconds during which time the Range Oscillator outputs 5 pulses. In a DOWN range situation, the DOWN range enable line goes low. This This signal is capacitively coupled by C3 to the gate of Q4 causing it to output one pulse. Five pulses counted by the Range Counter, located on the Display Assembly, commands a transition to the next higher range, while one pulse commands a transition to the next lower range. In either case, the first output pulse triggers the Range Delay One-Shot to allow the analog signal conditioners to settle in the new range.

Range Delay One-Shot Multivibrator

Transistors Q1 and Q2 make up the Range Delay One-Shot Multivibrator. A range change pulse from the Range Oscillator turns transistor Q2 ON and turns transistor Q1 OFF, placing

the One-Shot Multivibrator into its unstable state. The RC charge time of combined capacitors C2 and C6 and resistor R5 determine how long the One-Shot remains in its unstable state. With the filter selected, no current flows through R16 and the time out is about 220 milliseconds. When the filter is not selected, the time out is decreased to about 25 milliseconds because of the additional current path offered through R16 as a result of the SIGNAL 4 line potential which is established in the Display Assembly. The SIGNAL 3 line disables the Sample Command Oscillator during range delay time and SIGNAL 2 retriggers the Sample Command Oscillator at the end of the range delay time.

POWER SUPPLY (A1) Drawing No. 8400A-1100

The Power Supply consists of four regulating circuits supplying +18 and −18 volt operating supplies, a 200 volt supply for display tube ionization, and a 5 volt logic supply.

The +18 and −18 volt operating supplies are operated from the full-wave rectifiers consisting of diodes CR5 through CR8 and filter capacitors C2 and C5. The +18 volt regulator consists of operational amplifier U1 and series pass transistor Q3. The voltage reference for the +18 volt operating supply regulator is derived from reference amplifier U9 and a temperature compensation transistor located on the Logic assembly. The −18 volts is referenced to zener diode CR9.

The +200 volts regulator is operated from a full-wave rectifier and filter consisting of diodes CR1 through CR4 and capacitor C1. The reference for the +200 volts regulator is furnished by the +18 volt supply. Voltage variations are amplified in transistor Q2 and applied to the series pass transistor Q1.

The +5 volt regulator is operated from a full-wave rectifier and filter consisting of CR10 through CR13 and capacitor C8. The reference for the +5 volts regulator is taken from the −18 volts via a voltage divider formed by R14, R15, and R17. The series pass element is a compound emitter follower composed of transistor Q8 driving power transistor Q6. Voltage variations which are detected by the sample string R14, R15, and R17 are amplified by Q7.

AC CONVERTER −01 OPTION Drawing No. 8400A-1007

Operational Rectifier

Input FET Q1 functions as a source follower while transistor Q2 provides a low impedance guard voltage which is used to boot-strap most of the capacity that otherwise would appear between the gate and the circuit common. The first two differential pairs are in a dual in-line package U1, and together with Q4 and Q5 develop the required gain. Transistors Q3 and Q6 function as current sources with values such that clipping due to overload is symmetrical. Changes in capaciter charges are small and amplifier recovery time is minimized. Transistor Q7 compensates for capacitance losses in the diodes.

DC Difference Amplifier/Integrator

The filter network which provides the input to the Amplifier/Integrator consists of a multi-section RC filter matched in such a manner as to maintain a good Common Mode Rejection. Gain for the DC amplifier is provided by a monolithic operational amplifier U2 with a total open-loop gain of approximately 5 times 10^5.

Range and Function Control

The converter input and output relays K1 and K2 are operated from the VAC control lines. The range relays K4 through K6 are operated by driver circuitry consisting of NAND gates U4A, U4C, and U4D. These range control gates accept the Buffer output of the range counter. U3B and U4B deliver the UP and DOWN range stop commands for VAC function through the range delay assembly. The NAND gates U3A and U3C deliver the set and reset commands to the Range Counter for prevention of illegal or disallowed ranges in the volt AC function.

OHMS CONVERTER –02 OPTION Drawing No. 8400A-1010

The Ohms Converter is operated in one of two configurations associated with the functions of Ohms and Kilohms. In the Ohms function, the convertor is a constant current source which is connected to the terminals on the front panel of the 8400A. In KΩ function the Ohms Converter is the precision scaling resistor, which, in conjunction with the Buffer Amplifier located in the basic instrument, and the unknown resistor produces a voltage proportional to the unknown resistance.

Constant Current Generator

Regulated DC voltage is developed by resistors R2, R4, R5, zener diode CR3, Transistor Q1, and operational amplifier U1. The divider string R6, R7, and R8 scales the zener reference voltage and applies it to amplifier U2. Range resistors R10 through R16, in conjunction with zener CR3, apply a range dependent constant current to the emitter of Darlington pair composed of Q2 and Q3. Fuse F1 capacitor C6 and diodes CR2 and CR4 are used as an overvoltage protection circuit for the current generator.

Range Scaling Network

Resistors R17 through R22 and relay contacts K1A, K2A, and K4 are the Range-Scaling Network. Relay contacts K1A and K2A are actuated by range selection. Relay K4 is actuated in the KΩ function and connects one end of the scaling network to the high source terminal on the front panel.

Relay Drive Circuit

Range control relay K1 receives its call commands from the Buffer Assembly, whereas K2 receives its call commands from the Range Counter. Function control relays K3 and K4 are controlled by transistors Q5 and Q6. Our manual range condition is detected by gate U5E which enables gates U5C and U5D to control Q5 and Q6. In an autorange condition, gates U5C and U5D are disabled and function control is transferred by gate U3B to RS flip-flop U3A and U3C. Mutually exclusive outputs of this flip-flop in turn control switches Q5 and Q6. Gates U4A and U4B operate on the set and reset lines of the RS flip-flop to enable an automatic change of function in an autorange condition.

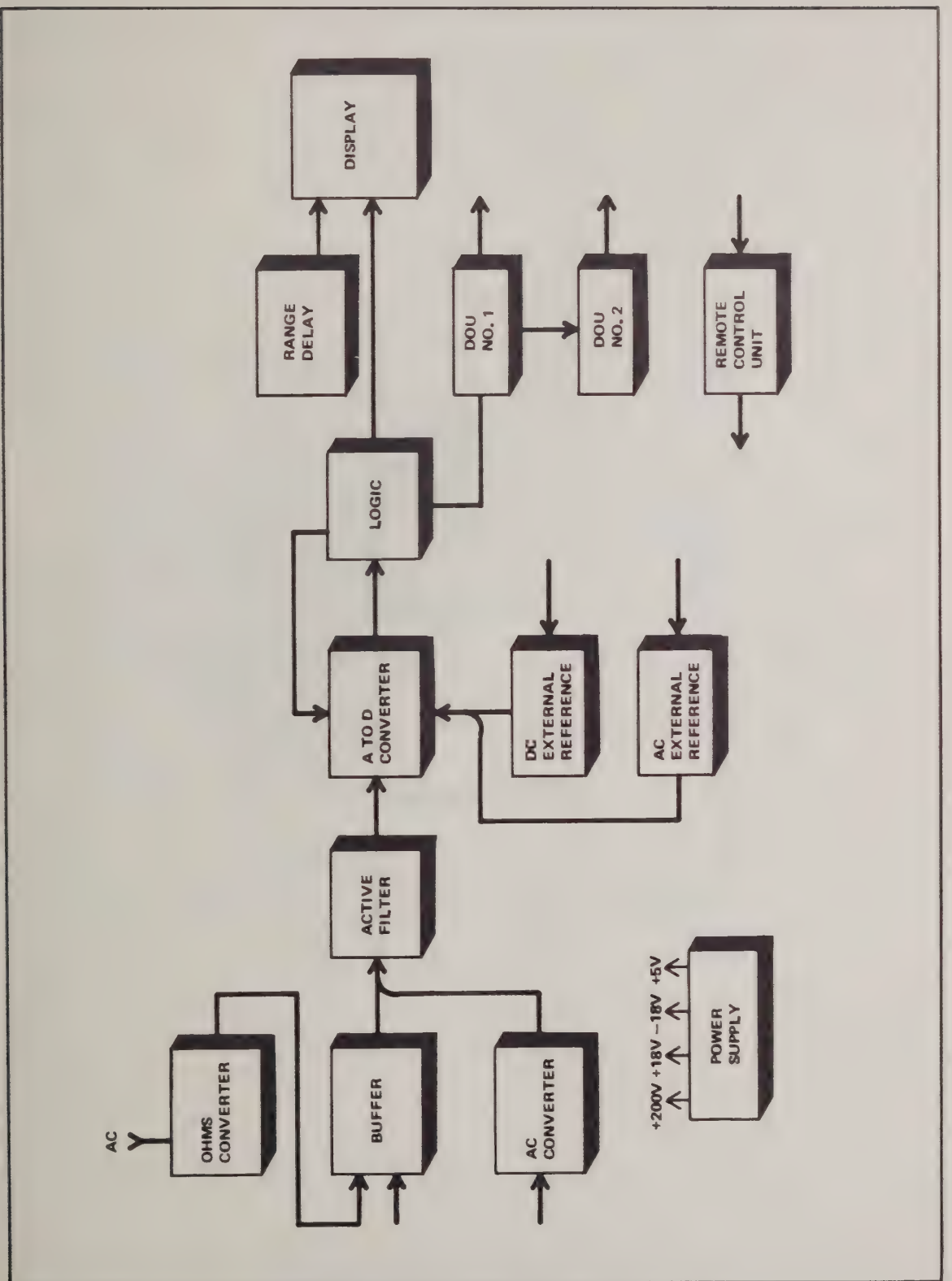


FIGURE 1. MODEL 8400A BLOCK DIAGRAM

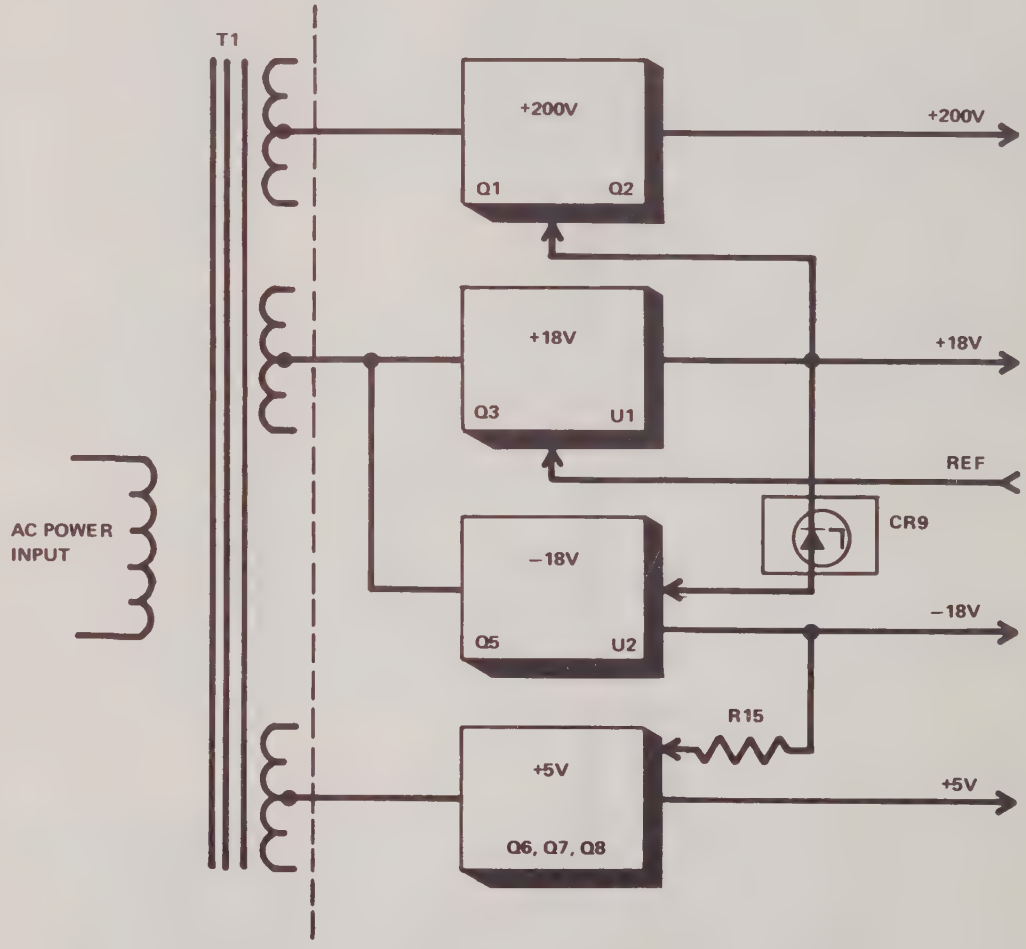


FIGURE 2. A1 POWER SUPPLY

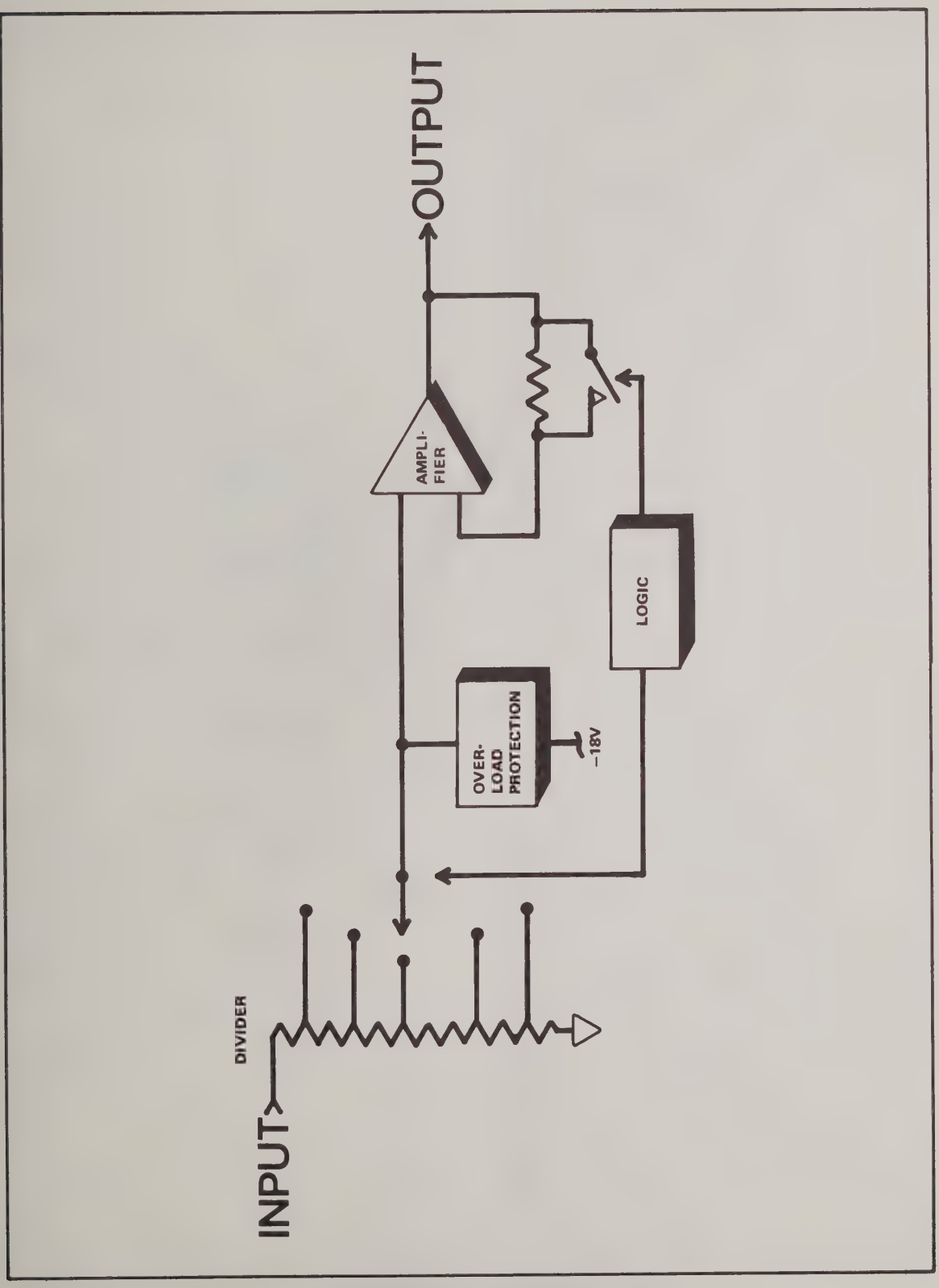


FIGURE 3. A11 BUFFER

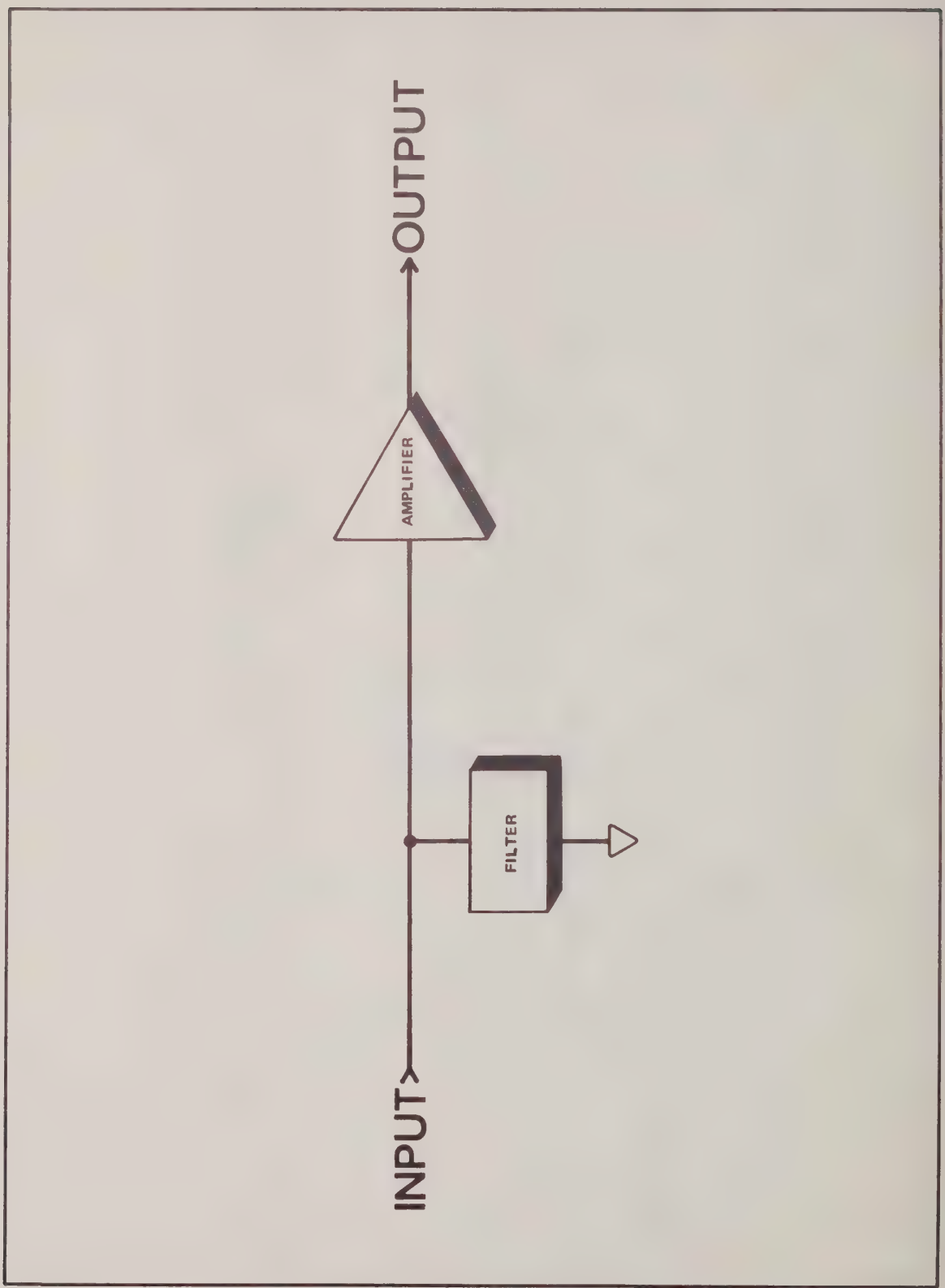


FIGURE 4. A10 ACTIVE FILTER

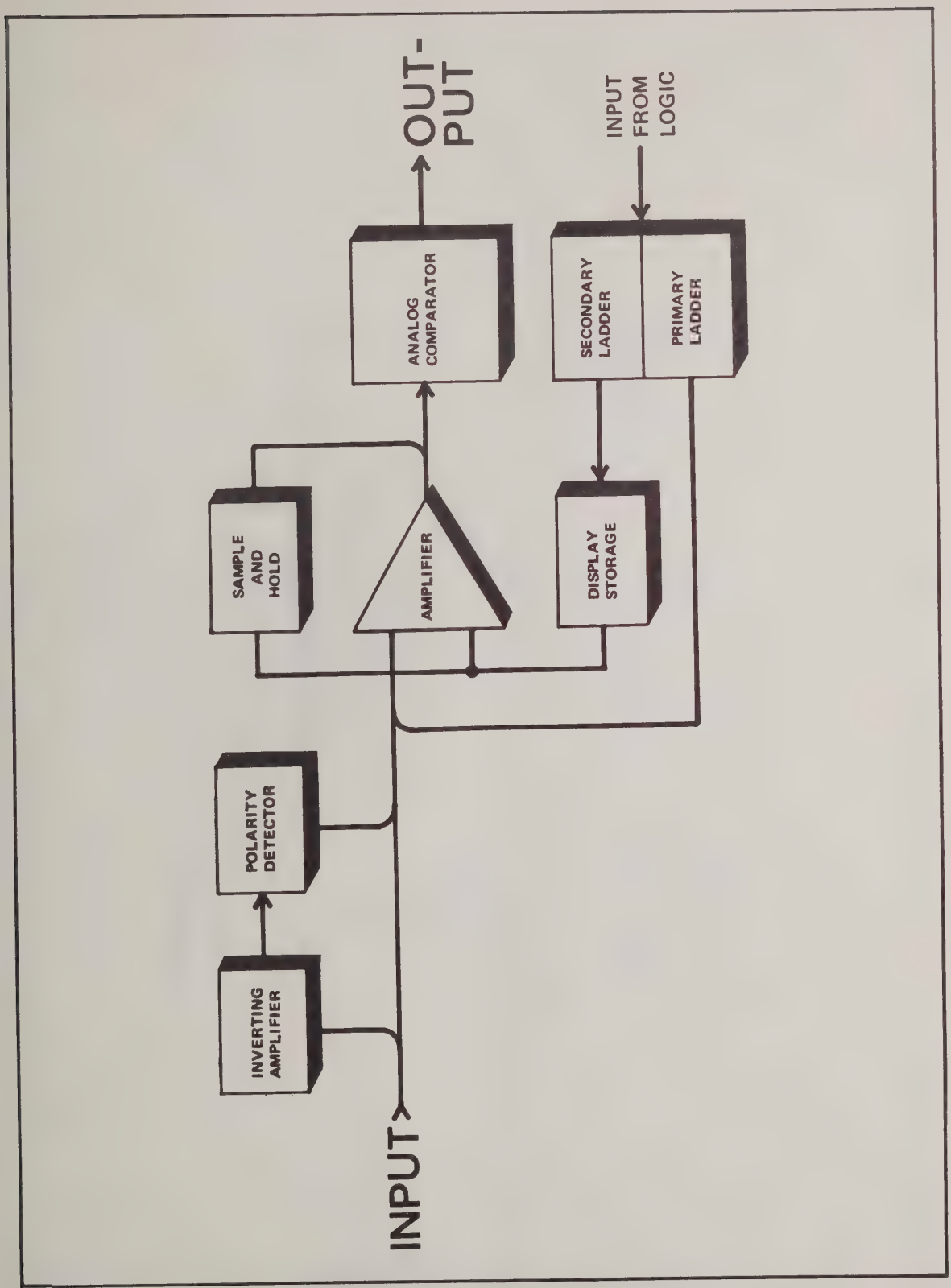


FIGURE 5. A9 A-TO-D CONVERTER

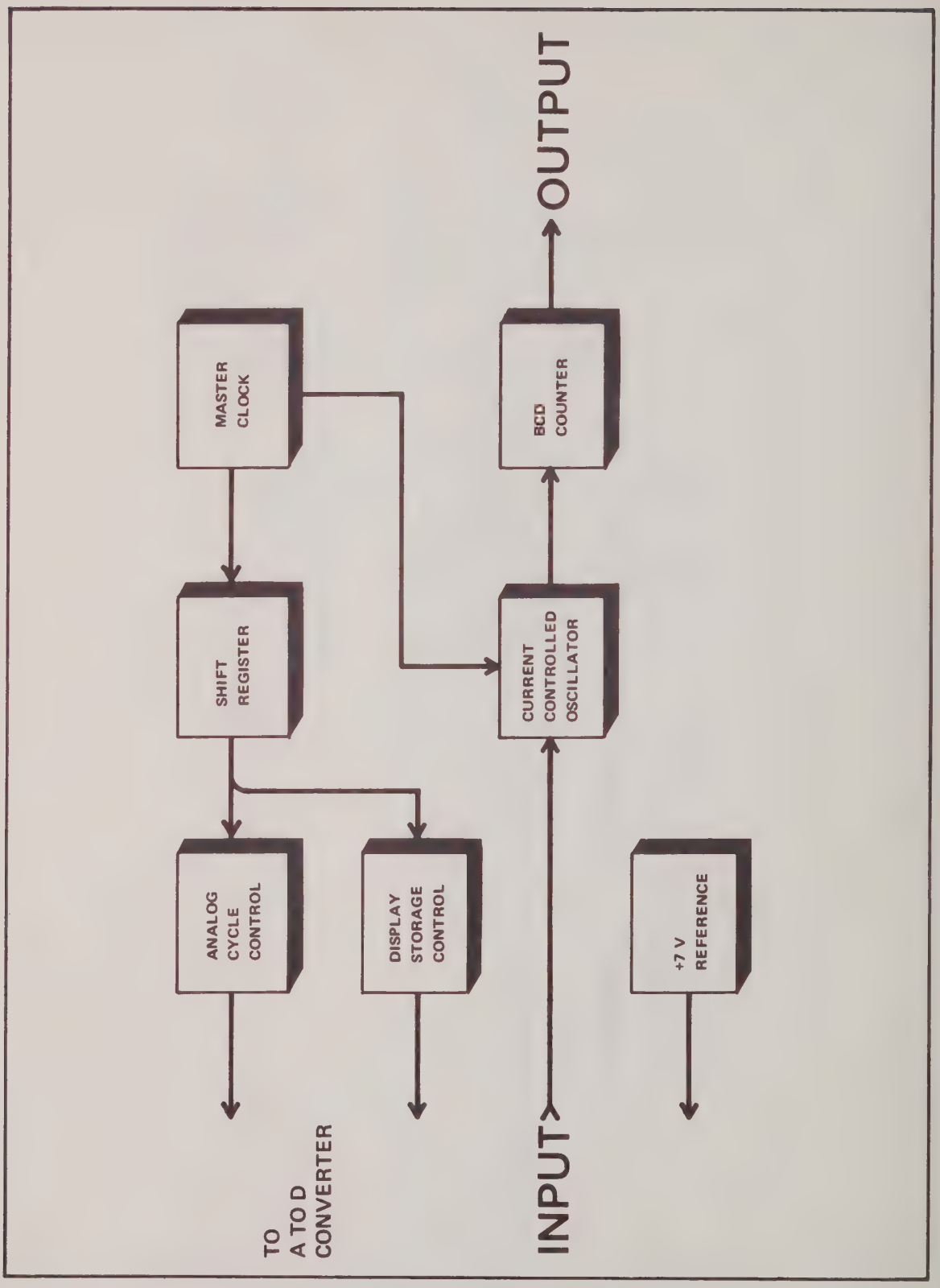


FIGURE 6. A8 LOGIC

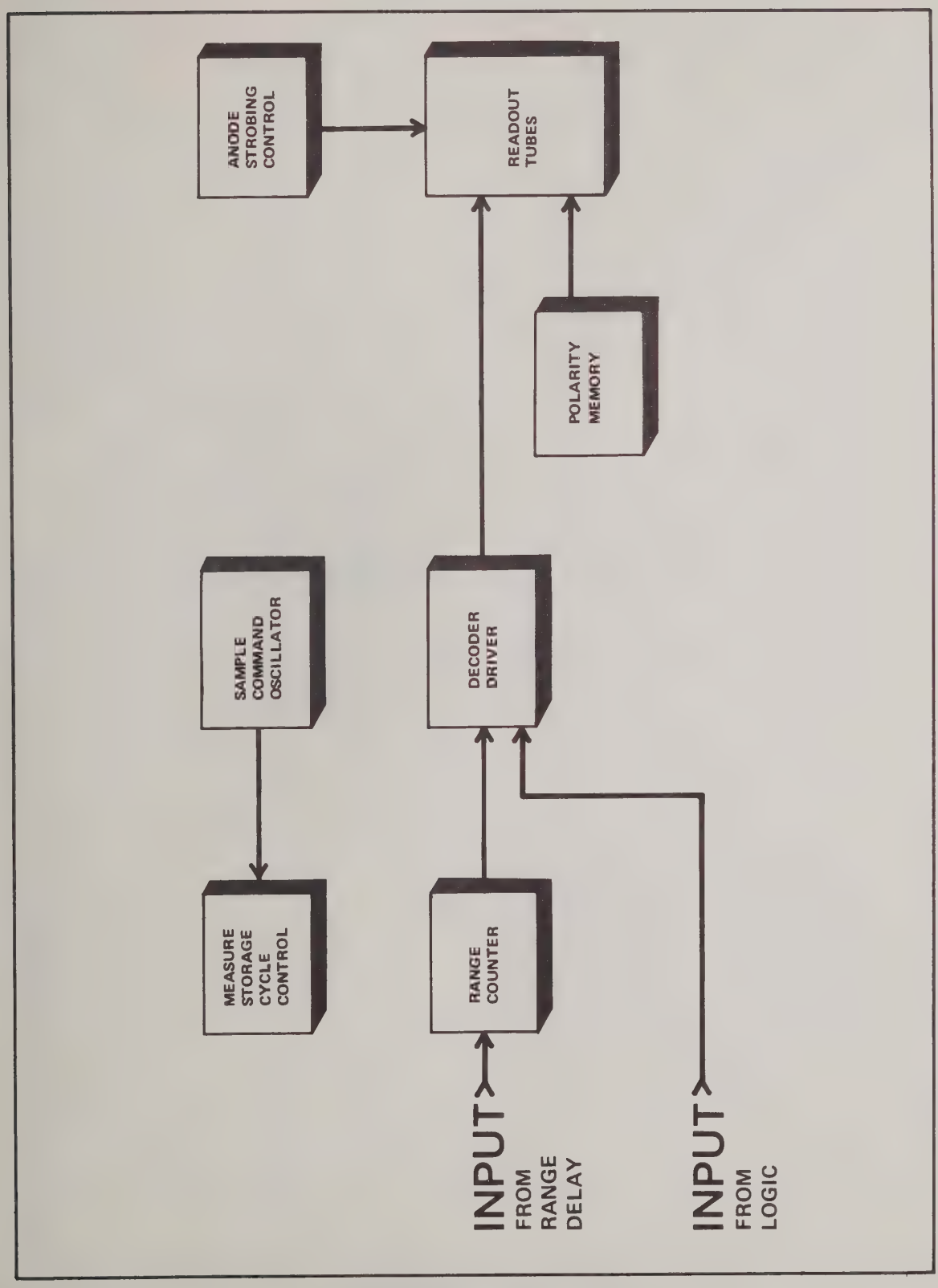


FIGURE 7. A14 DISPLAY

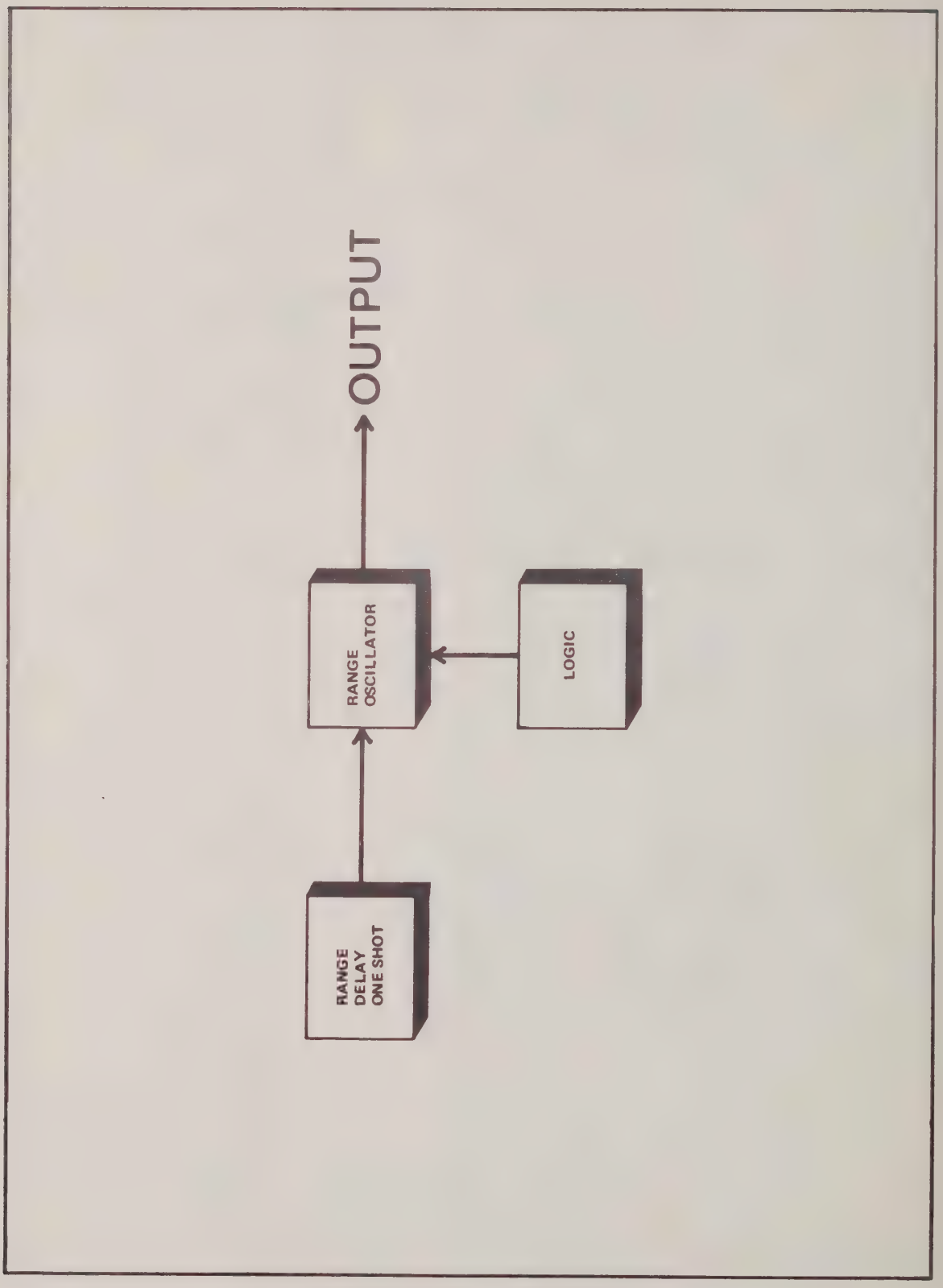


FIGURE 8. A2 RANGE DELAY

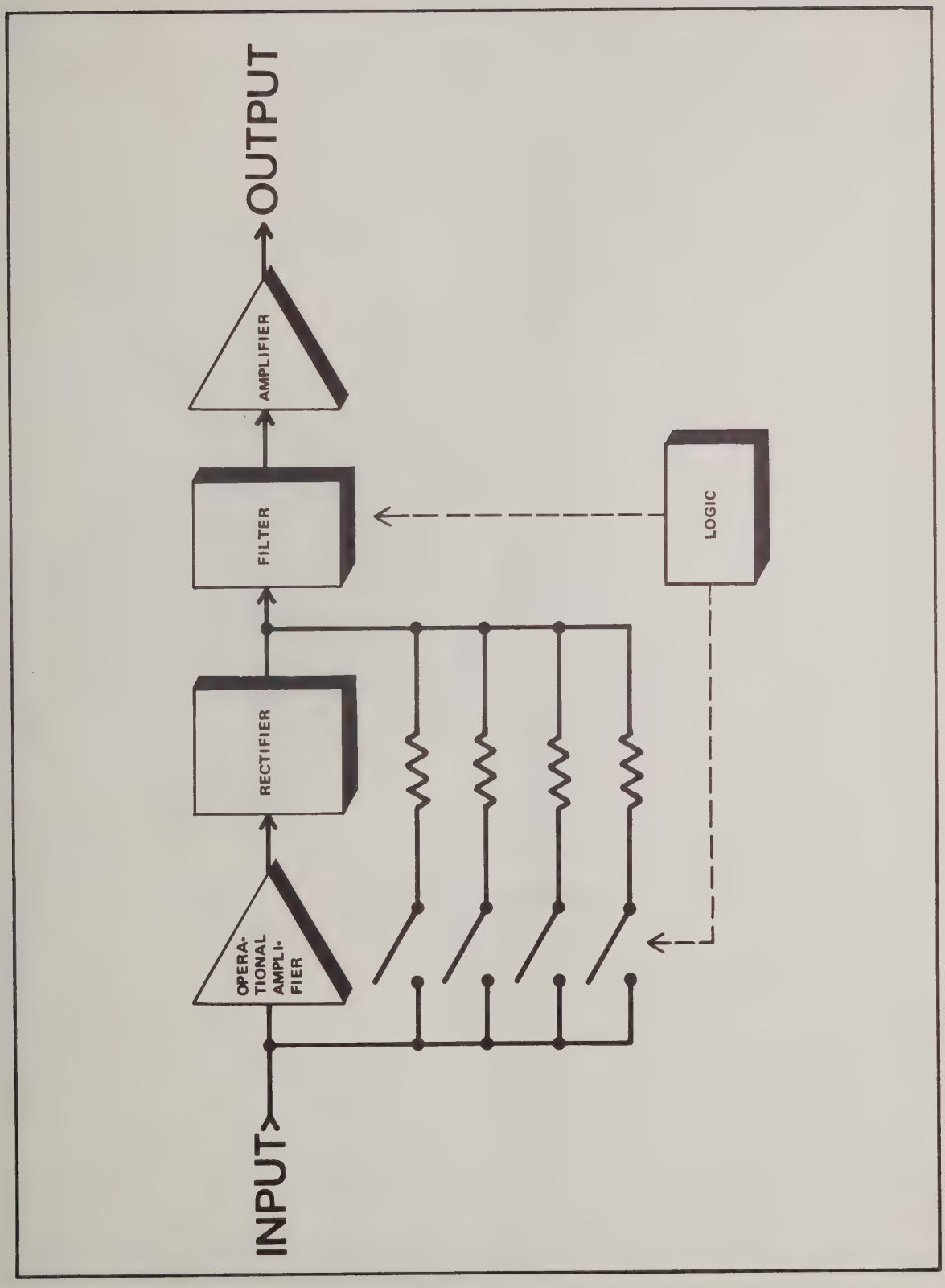


FIGURE 9. A13 AC CONVERTER

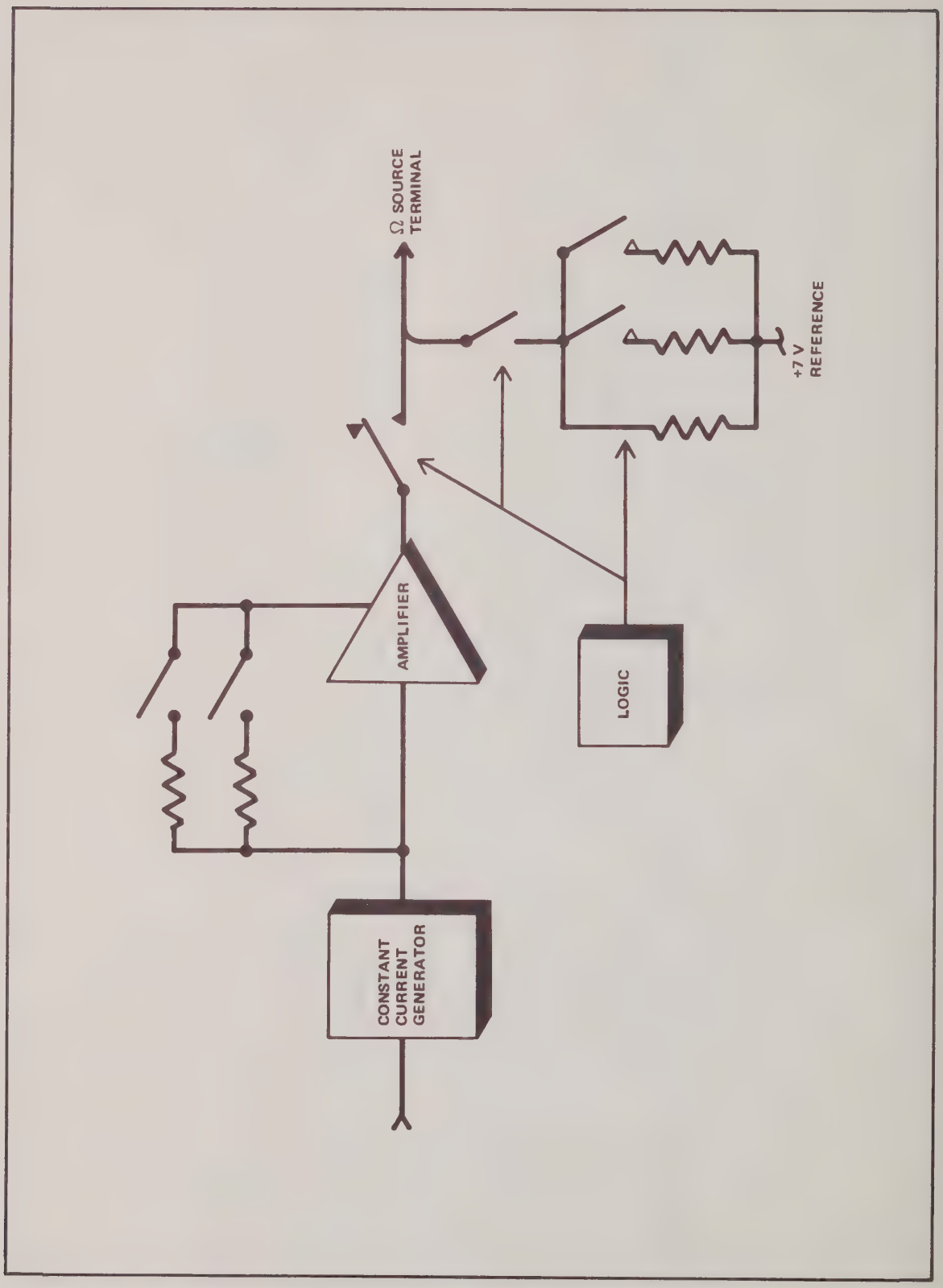


FIGURE 10. A12 OHMS CONVERTER

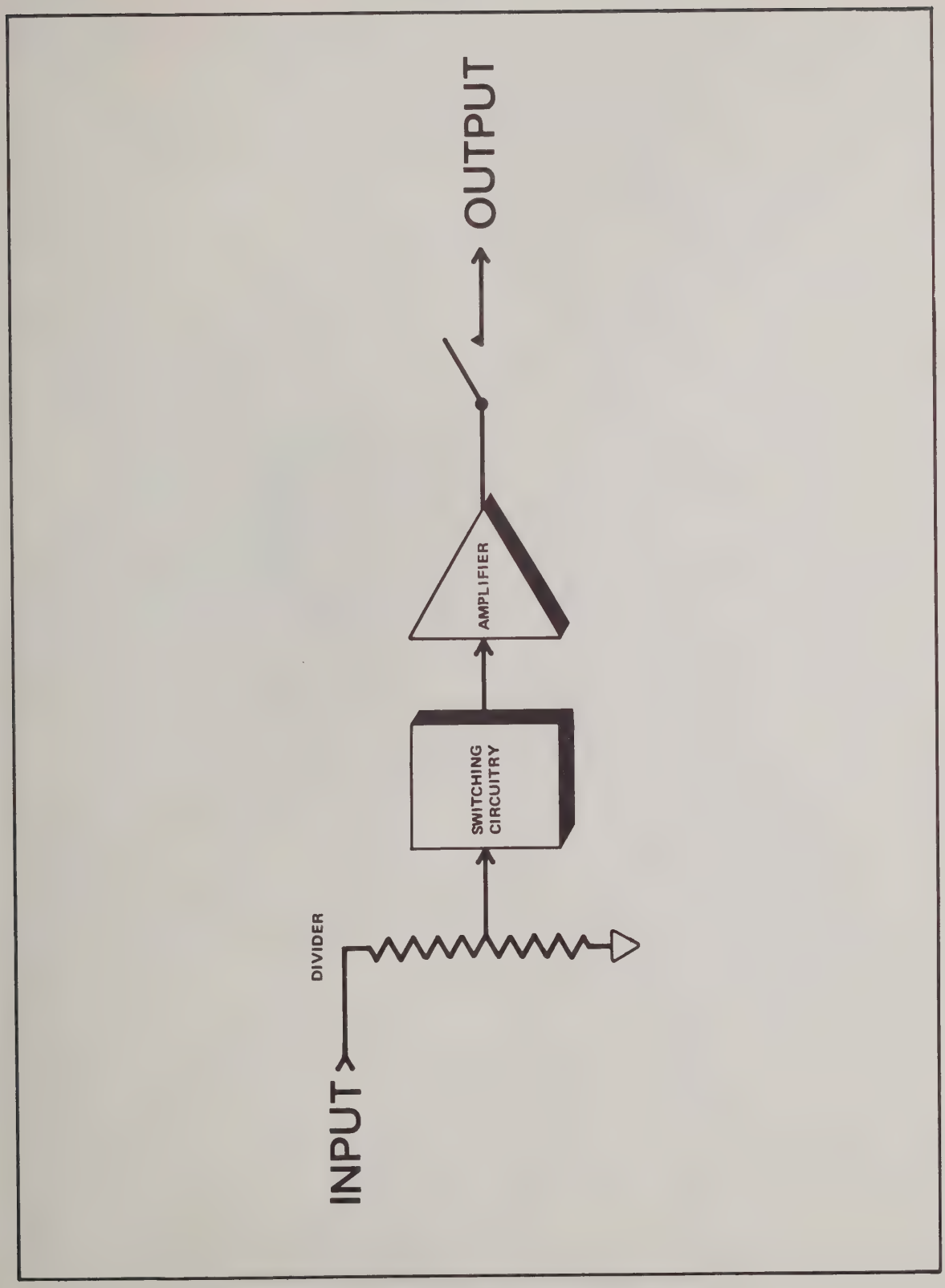


FIGURE 11. A3 DC EXTERNAL REFERENCE

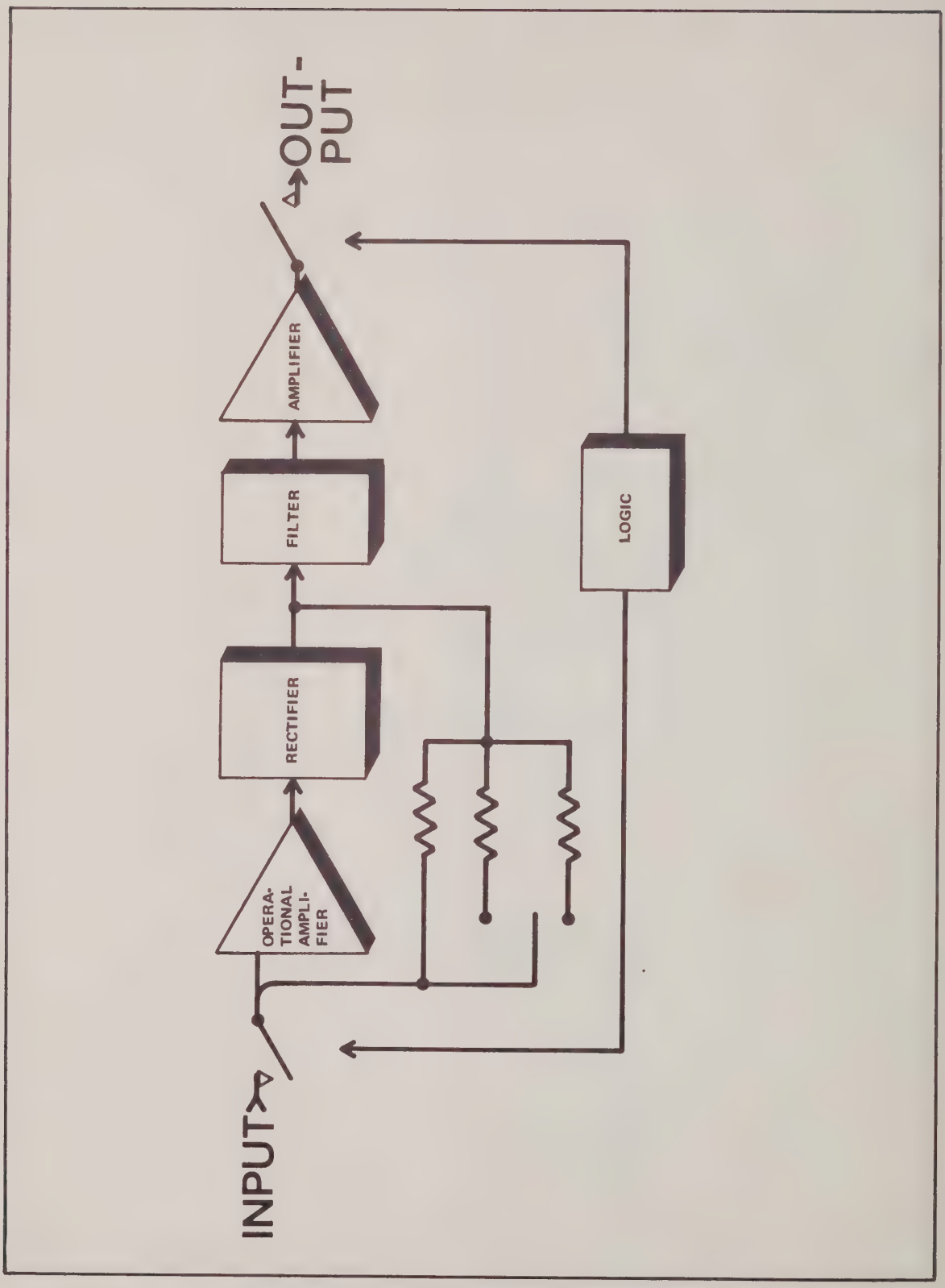
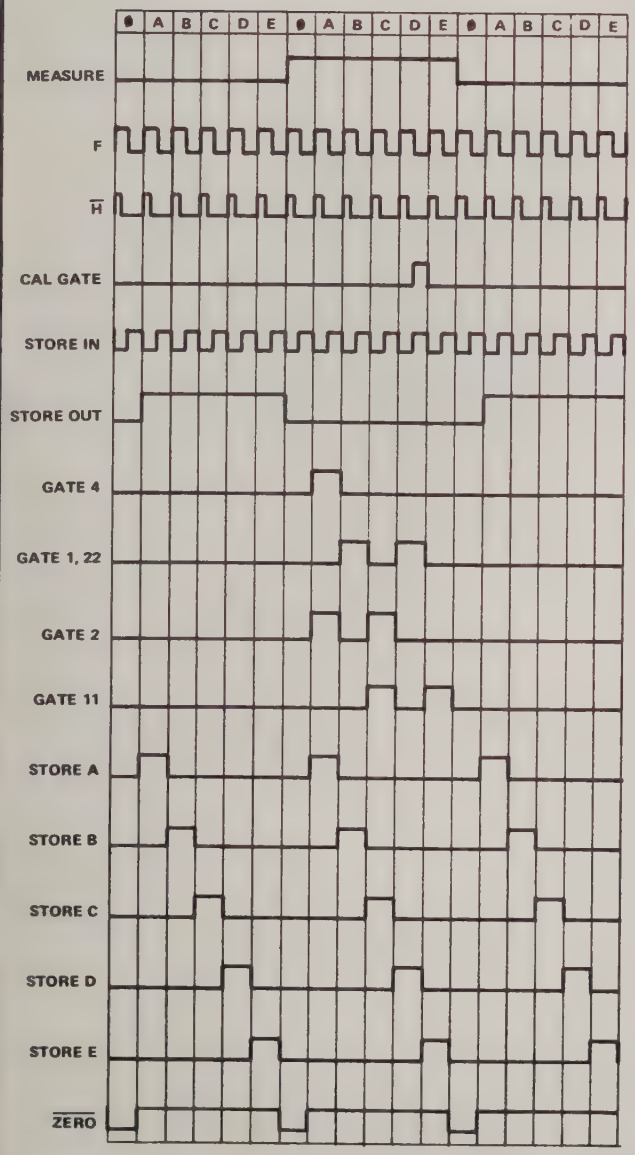


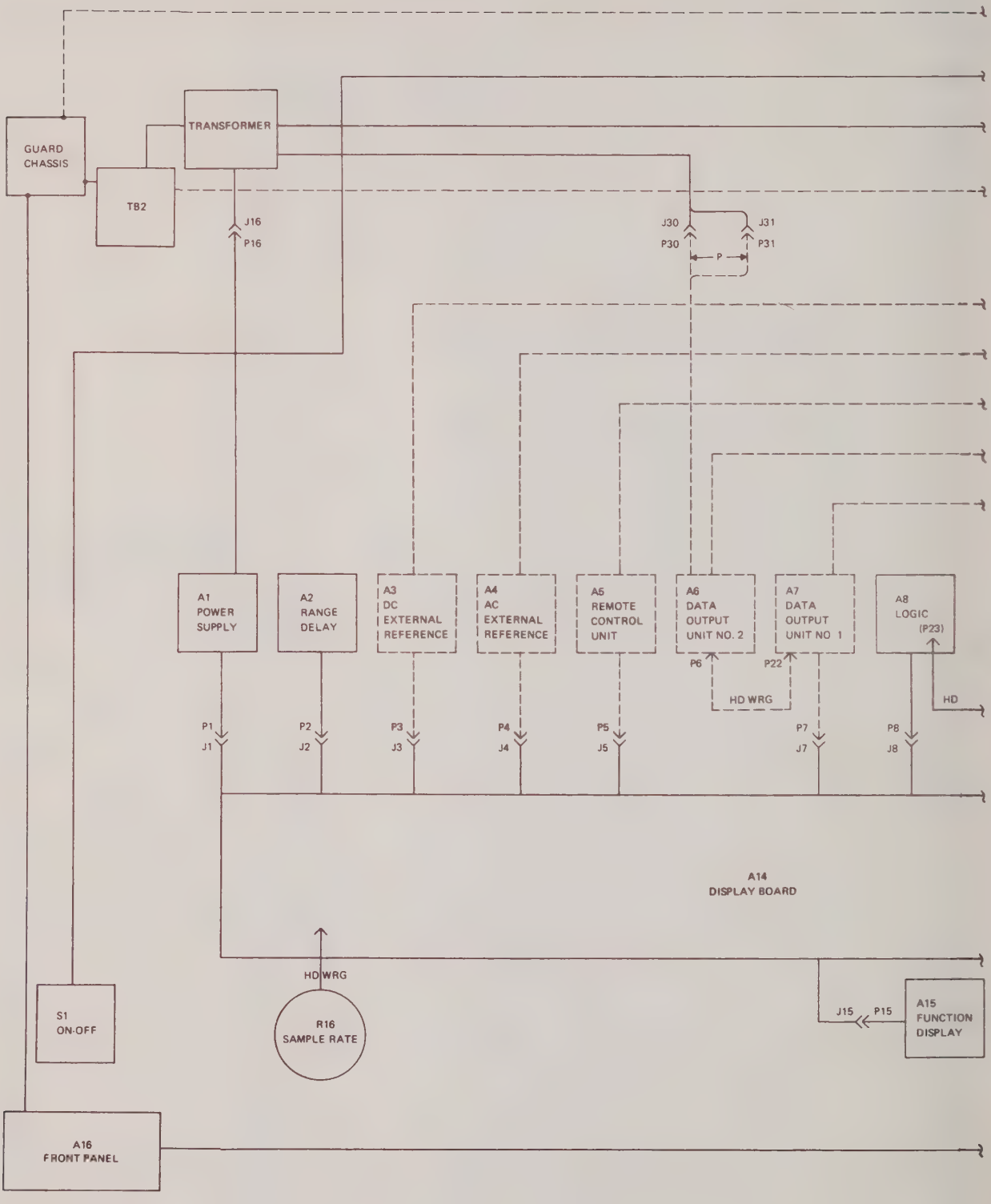
FIGURE 12. A4 AC EXTERNAL REFERENCE

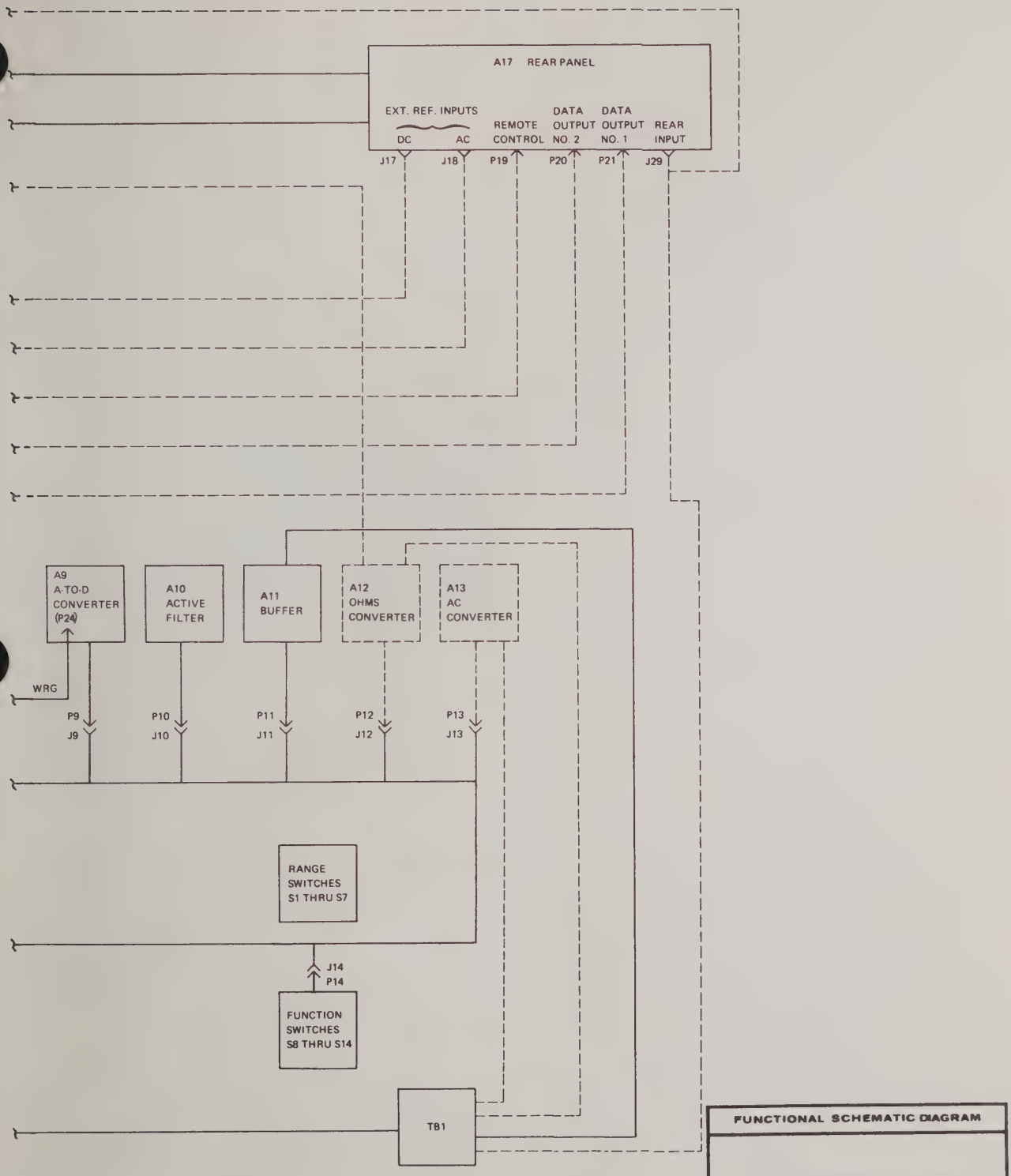
SUBPERIOD	SHIFT REGISTER FLIP FLOP AND ZERO GATE OUTPUT STATES					
	U3B	U3A	U4A	U4B	U1A	U2B
ZERO	0	0	0	0	0	0
A	1	0	0	0	0	1
B	0	1	0	0	0	1
C	0	0	1	0	0	1
D	0	0	0	1	0	1
E	0	0	0	0	1	1



CCO PULSE COUNT	SIXTEEN - STATE BINARY COUNTER			
	U5B Z	U5A Y	U6A X	U6B W
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	0	1	1
14	0	1	1	1
15	1	1	1	1

FIGURE 13. COUNTING CIRCUIT

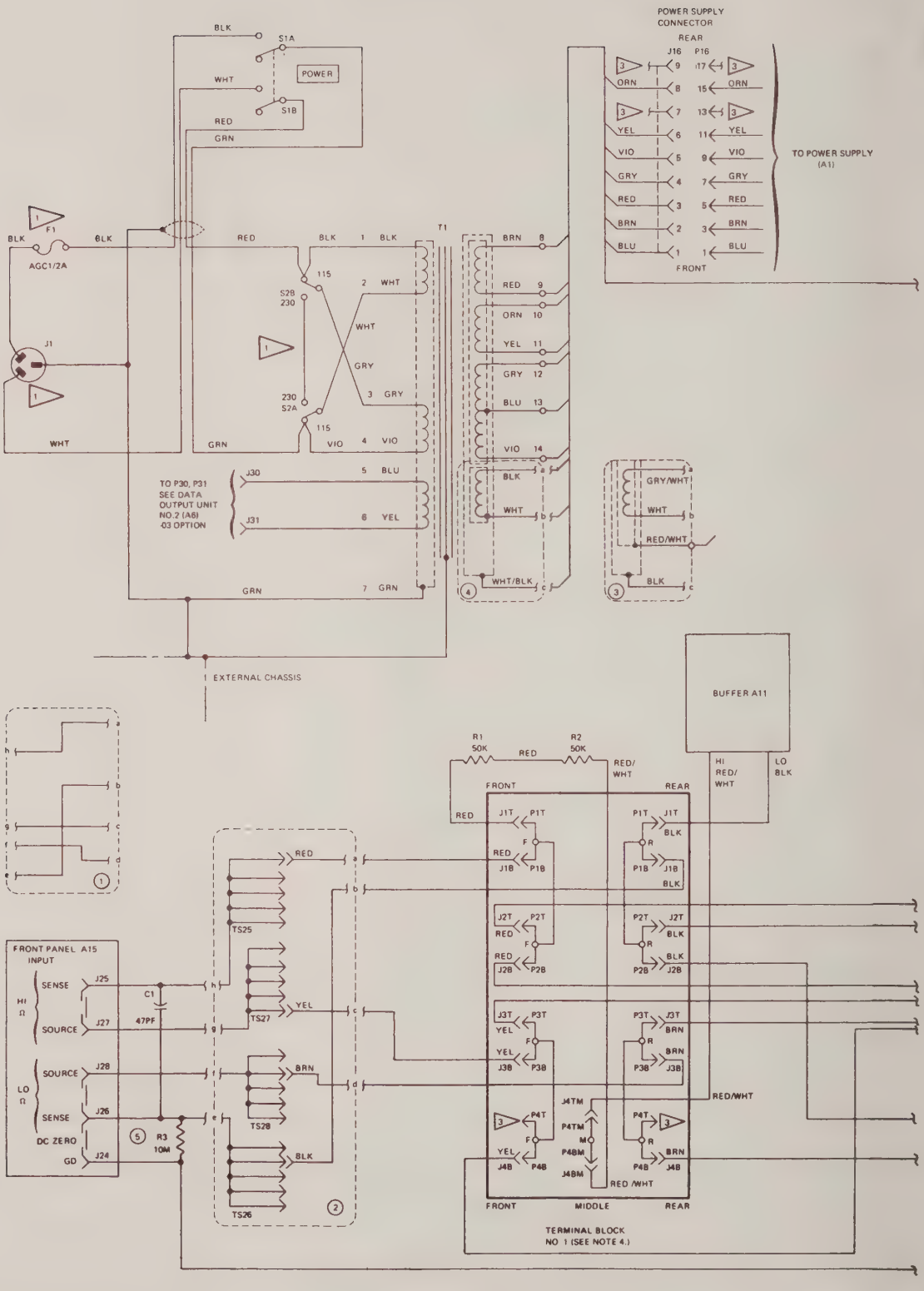

GUARD CHASSIS
TRANSFORMER
TB2
J16
P16
J30
P30
P
J31
P31
A1 POWER SUPPLY
A2 RANGE DELAY
A3 DC EXTERNAL REFERENCE
A4 AC EXTERNAL REFERENCE
A5 REMOTE CONTROL UNIT
A6 DATA OUTPUT UNIT NO. 2
A7 DATA OUTPUT UNIT NO 1
A8 LOGIC (P23)
P6
P22
HD WRG
HD
P1
J1
P2
J2
P3
J3
P4
J4
P5
J5
P7
J7
P8
J8
A14 DISPLAY BOARD
HD WRG
S1 ON-OFF
R16 SAMPLE RATE
J15
P15
A15 FUNCTION DISPLAY
A16 FRONT PANEL

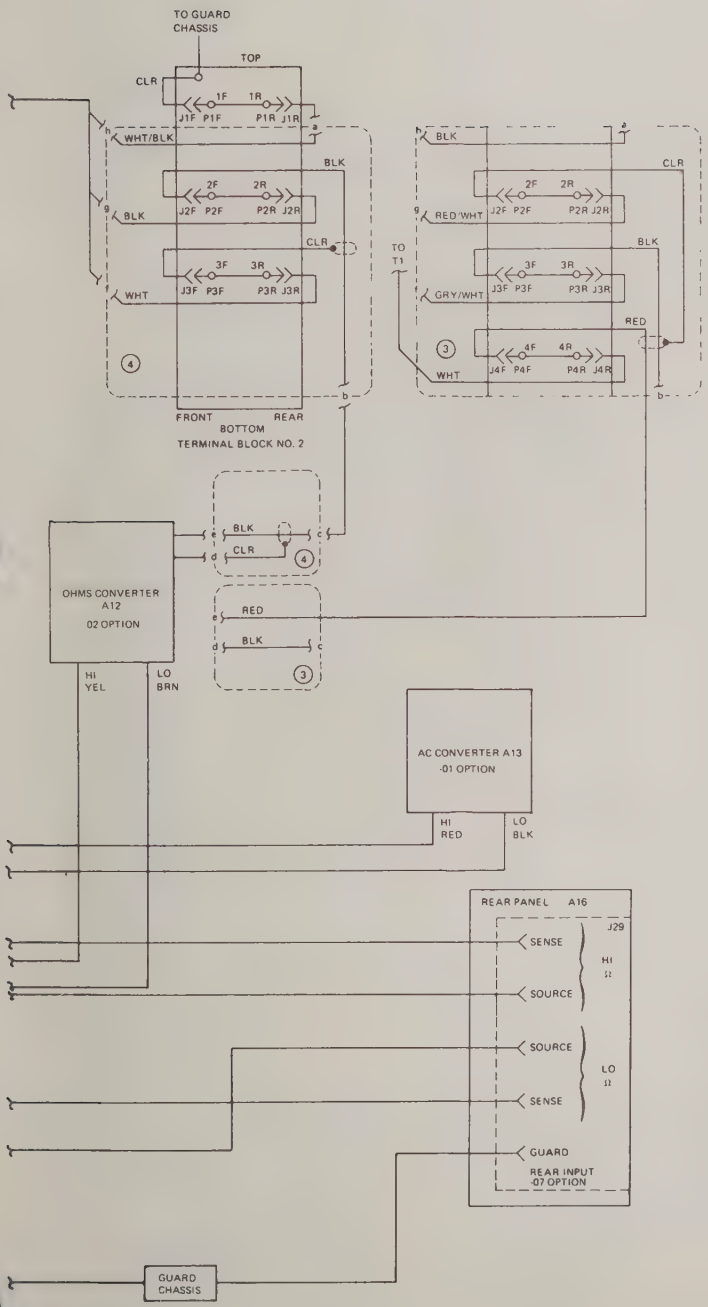


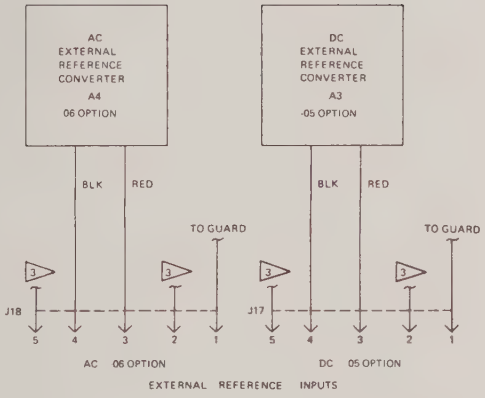
NOTES:

1. HD WRG — HARD WIRING NOT TO BE DISCONNECTED.
2. - - - — CONNECTIONS FOR OPTIONS.

FUNCTIONAL SCHEMATIC DIAGRAM	
INTERCONNECT DIAGRAM	
8400A-1100	REV. —
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


POWER SUPPLY CONNECTOR
REAR
J16 P16
TO POWER SUPPLY (A1)
FRONT
BLK
S1A
POWER
WHT
S1B
RED
GRN
F1
AGC1/2A
J1
WHT
T1
115
230
S2B
S2A
TO P30, P31 SEE DATA OUTPUT UNIT NO.2 (A6) 03 OPTION
J30
J31
EXTERNAL CHASSIS
BUFFER A11
R1 50K
R2 50K
HI RED/ WHT
LO BLK
FRONT PANEL A15 INPUT
SENSE
SOURCE
DC ZERO
GD
C1 47PF
R3 10M
TS25
TS27
TS28
TS26
FRONT
MIDDLE
REAR
TERMINAL BLOCK NO 1 (SEE NOTE 4.)





NOTES

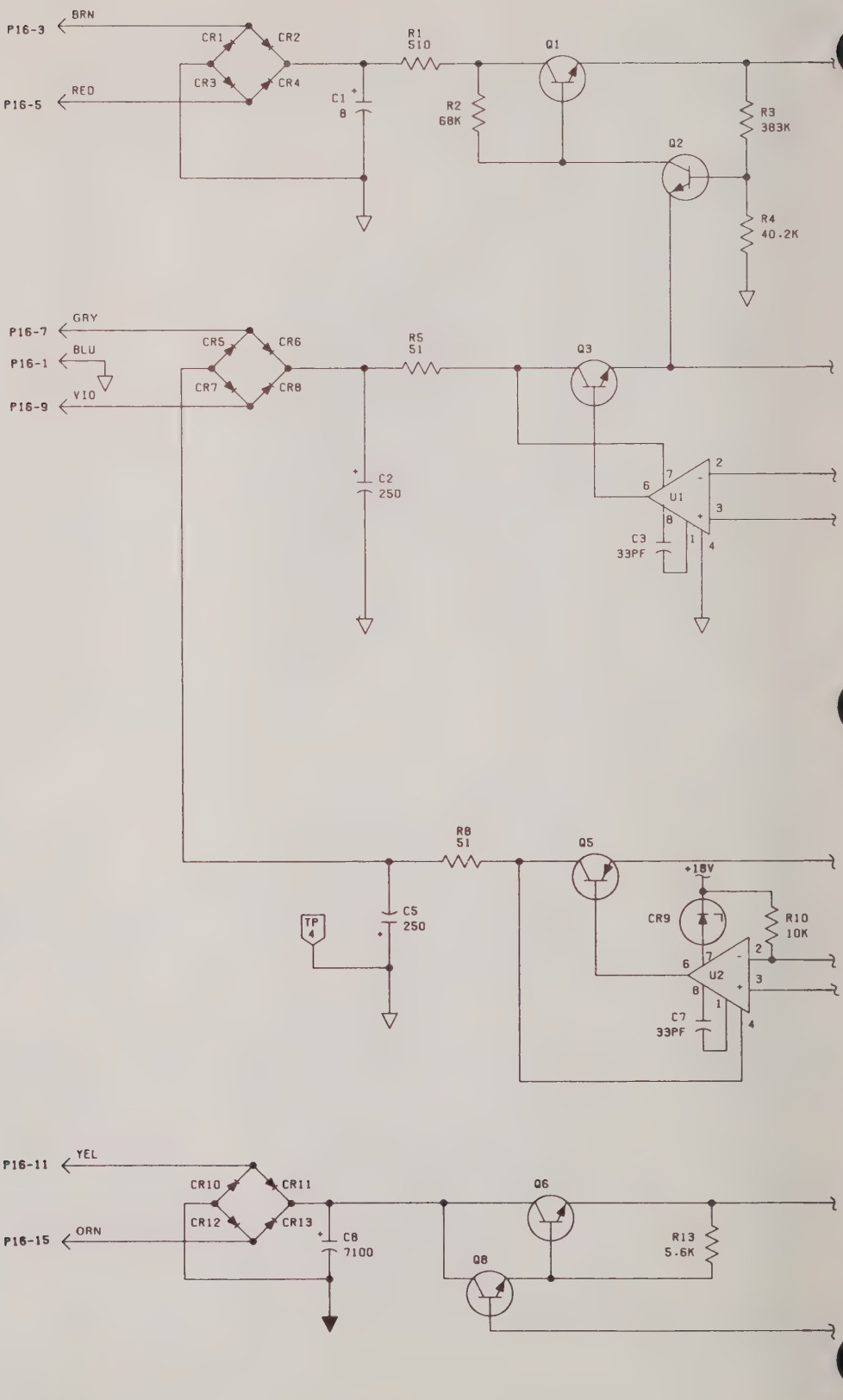
1. ALL RESISTANCES IN OHMS UNLESS OTHERWISE SPECIFIED
2. DENOTES FRONT PANEL LOCATION
3. NOT USED
4. 1T, FO, 1B — INDICATES LEFT MOST (1ST) DUAL PLUG CONNECTOR EXTENDING THRU TOP (T) AND BOTTOM (B) OF TERMINAL BLOCK IN FRONT (F) ROW
5. F1, J1, AND S2 LOCATED ON REAR PANEL

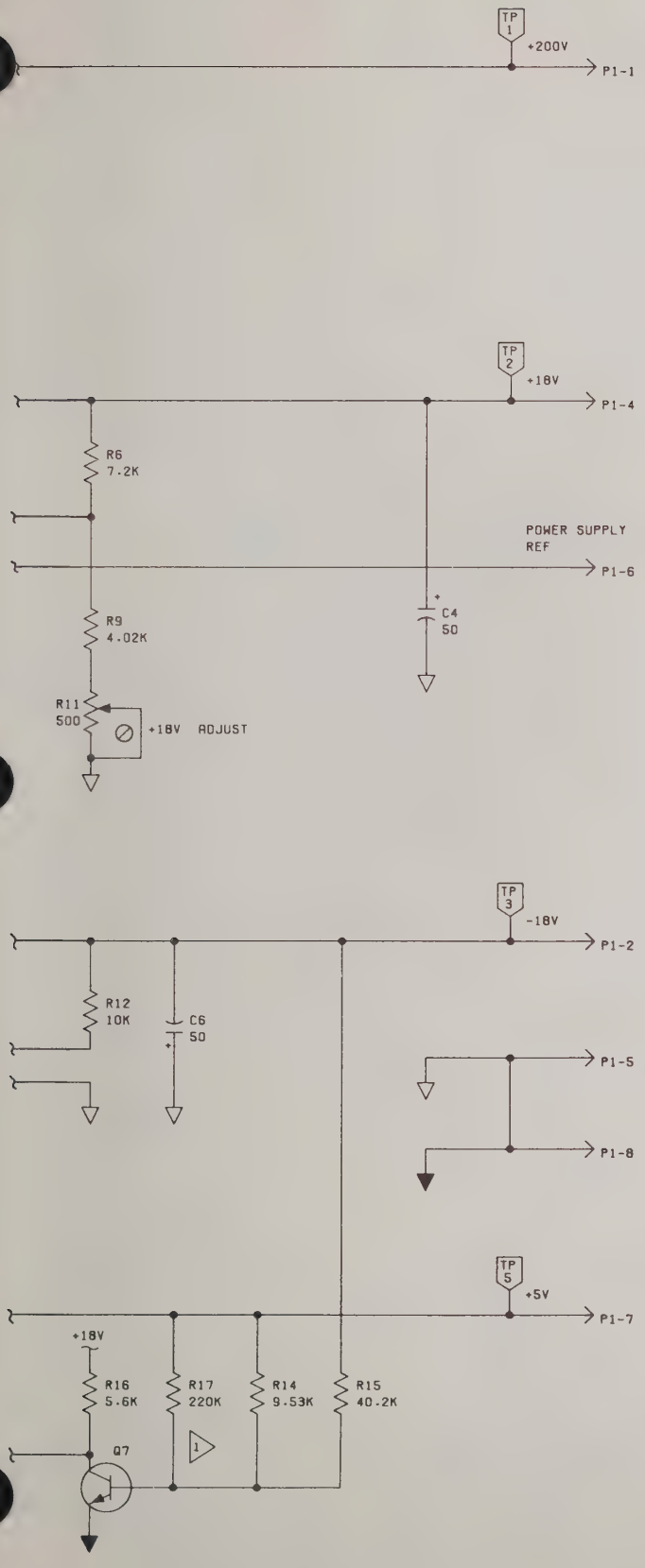
CHANGES

(1) SERIAL NO. 197 AND BELOW
(2) SERIAL NO 198 AND ABOVE
(3) SERIAL NO 261 AND BELOW
(4) SERIAL NO 262 AND ABOVE
(5) R3 ADDED SERIAL NO 187 AND ABOV

FUNCTIONAL SCHEMATIC DIAGRAM	
WIRING DIAGRAM	
8400A-1000	REV b

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133

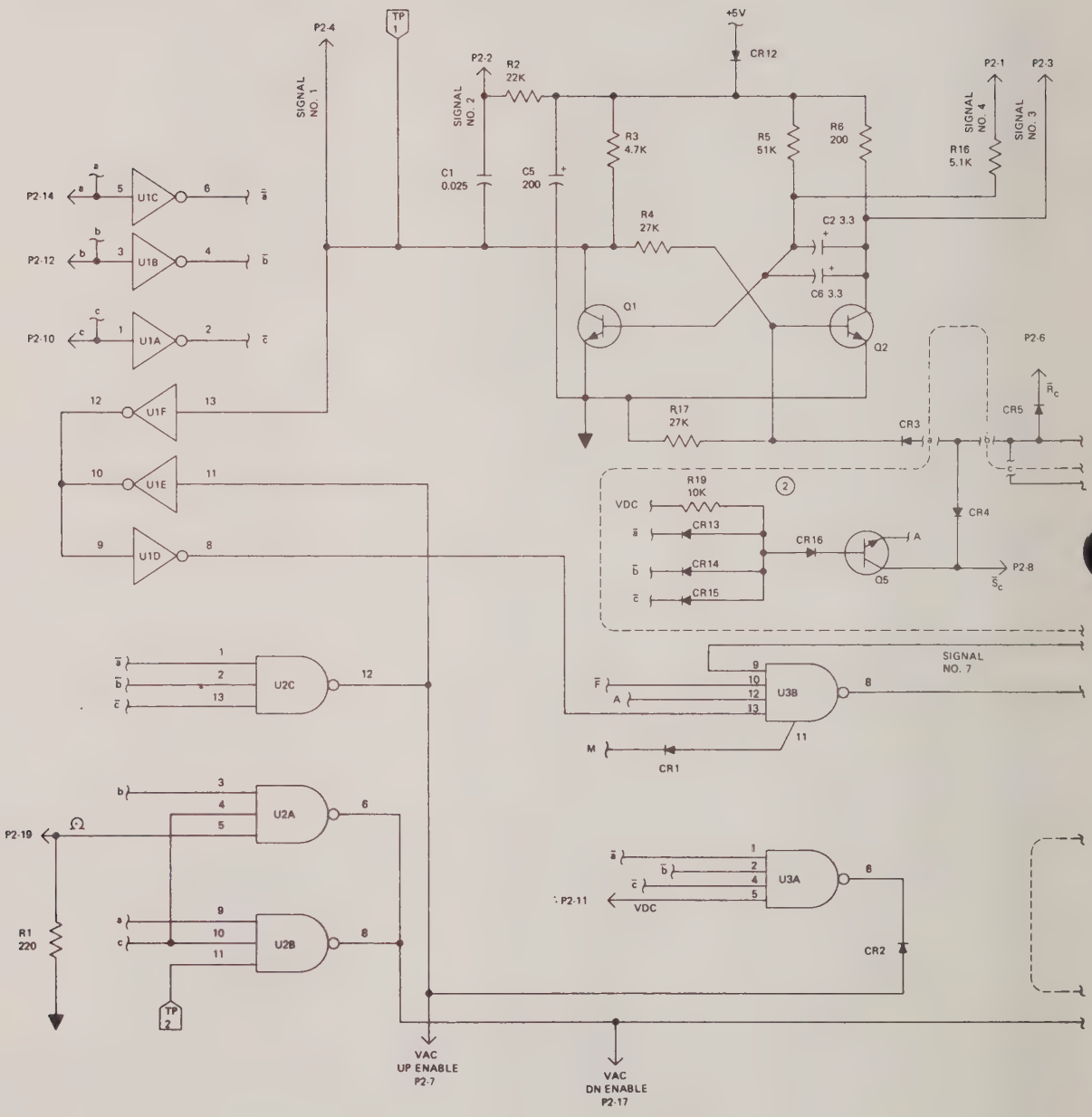

P16-3
BRN
P16-5
RED
CR1
CR2
CR3
CR4
C1
8
R1
510
R2
68K
Q1
Q2
R3
383K
R4
40.2K
P16-7
GRY
P16-1
BLU
P16-9
VIO
CR5
CR6
CR7
CR8
R5
51
Q3
C2
250
U1
C3
33PF
R8
51
Q5
TP
4
C5
250
+18V
CR9
R10
10K
U2
C7
33PF
P16-11
YEL
P16-15
ORN
CR10
CR11
CR12
CR13
C8
7100
Q6
Q8
R13
5.6K

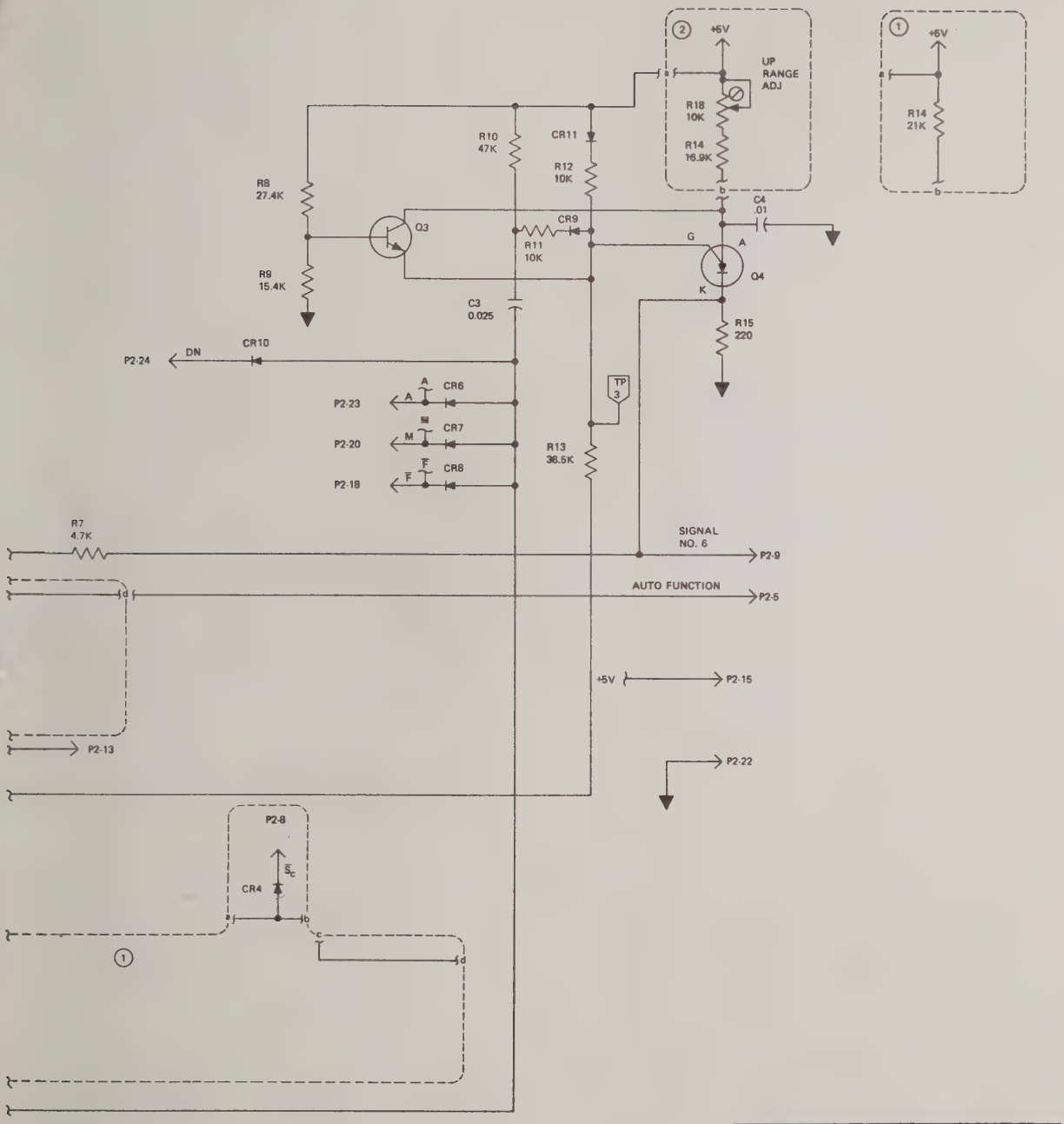


NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON.
3. ▼ DENOTES LOGIC COMMON.
4. ⊘ DENOTES INTERNAL ADJUSTMENT.
5. (1) R17 MAY BE OMITTED DURING ADJUSTMENT OF +5V SUPPLY.

FUNCTIONAL SCHEMATIC DIAGRAM	
A1 POWER SUPPLY	
8400A–1001	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


P2-4
TP 1
SIGNAL NO. 1
P2-2
SIGNAL NO. 2
R2 22K
+5V
CR12
P2-1
P2-3
SIGNAL NO. 4
SIGNAL NO. 3
R16 5.1K
R3 4.7K
R5 51K
R6 200
C1 0.025
C5 200
R4 27K
C2 3.3
C6 3.3
Q1
Q2
P2-14
P2-12
P2-10
U1C
U1B
U1A
U1F
U1E
U1D
R17 27K
CR3
CR5
P2-6
R19 10K
VDC
CR13
CR14
CR15
CR16
CR4
Q5
P2-8
SIGNAL NO. 7
U2C
U3B
M
CR1
U2A
U2B
P2-19
R1 220
TP 2
U3A
P2-11
CR2
VAC UP ENABLE P2-7
VAC DN ENABLE P2-17



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⏚ DENOTES LOGIC COMMON
3. ⊘ DENOTES INTERNAL ADJUSTMENT

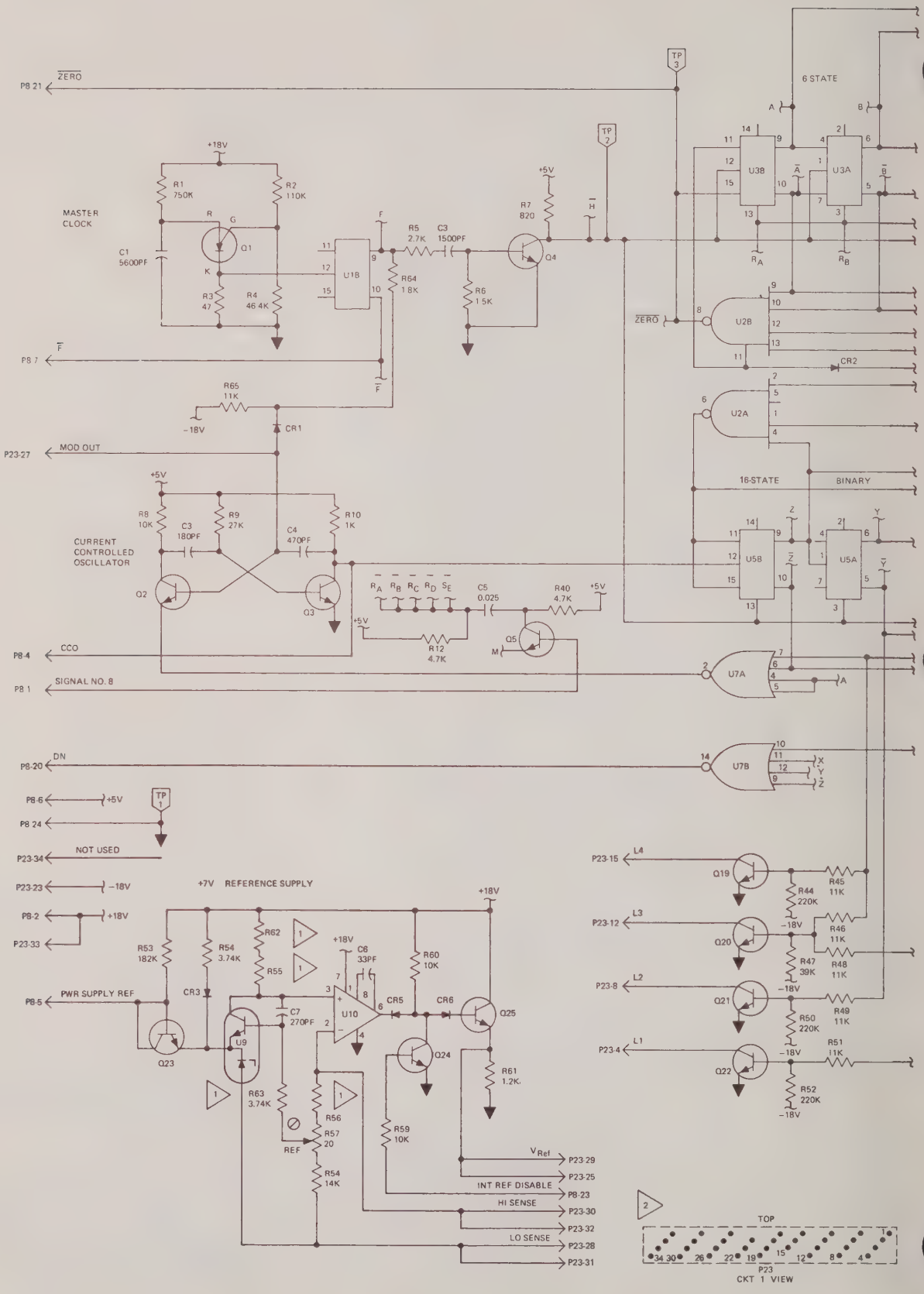
IC	PIN CONNECTIONS	
	+5V	COMMON
U1	14	7
U2	14	7
U3	14	7

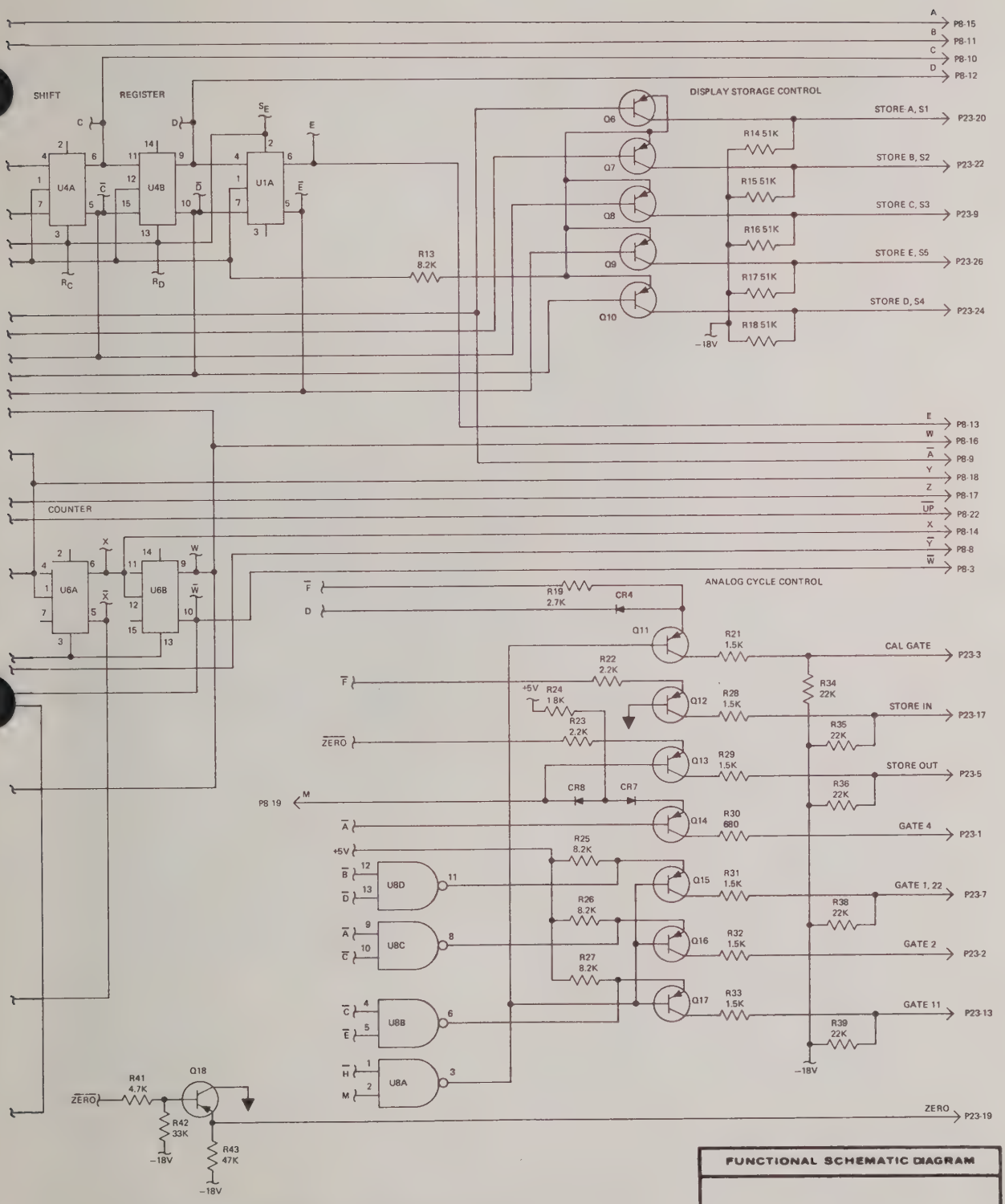
CHANGES

(1) SERIAL NO. 264 AND BELOW

(2) SERIAL NO. 265 AND ABOVE

FUNCTIONAL SCHEMATIC DIAGRAM	
A2 RANGE DELAY	
8400A–1006	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


P8 21 ZERO
TP 3
6 STATE
A
B
+18V
R1 750K
R2 110K
MASTER CLOCK
R
G
Q1
C1 5600PF
K
R3 47
R4 46.4K
U1B
F
R5 2.7K
C3 1500PF
R64 1.8K
R6 1.5K
+5V
R7 820
Q4
TP 2
H
U3B
U3A
R_A
R_B
ZERO
U2B
CR2
P8 7 F
F
R65 11K
-18V
CR1
U2A
P23-27 MOD OUT
16-STATE
BINARY
+5V
R8 10K
C3 180PF
R9 27K
C4 470PF
R10 1K
CURRENT CONTROLLED OSCILLATOR
Q2
Q3
U5B
U5A
R_A R_B R_C R_D S_E
C5 0.025
R40 4.7K
+5V
R12 4.7K
Q5
M
P8-4 CCO
P8 1 SIGNAL NO. 8
U7A
P8-20 DN
U7B
P8-6 +5V
TP 1
P8 24
P23-34 NOT USED
P23-23 -18V
+7V REFERENCE SUPPLY
P8-2 +18V
P23-33
R53 182K
R54 3.74K
R62
R55
+18V
C6 33PF
R60 10K
P8-5 PWR SUPPLY REF
CR3
C7 270PF
U10
CR5
CR6
Q25
Q23
U9
Q24
R61 1.2K
R63 3.74K
R56
R57 20
REF
R59 10K
R54 14K
V_Ref P23-29
INT REF DISABLE P8-23
HI SENSE P23-30
P23-32
LO SENSE P23-28
P23-31
P23-15 L4
Q19
R44 220K
R45 11K
P23-12 L3
Q20
R46 11K
R47 39K
R48 11K
P23-8 L2
Q21
R49 11K
R50 220K
P23-4 L1
Q22
R51 11K
R52 220K
TOP
34 30 26 22 19 15 12 8 4
P23
CKT 1 VIEW



1C	PIN CONNECTIONS	
	+5V	COMMON
U1, U3 U6	16	8
U2, U8	14	7
U7	8	1

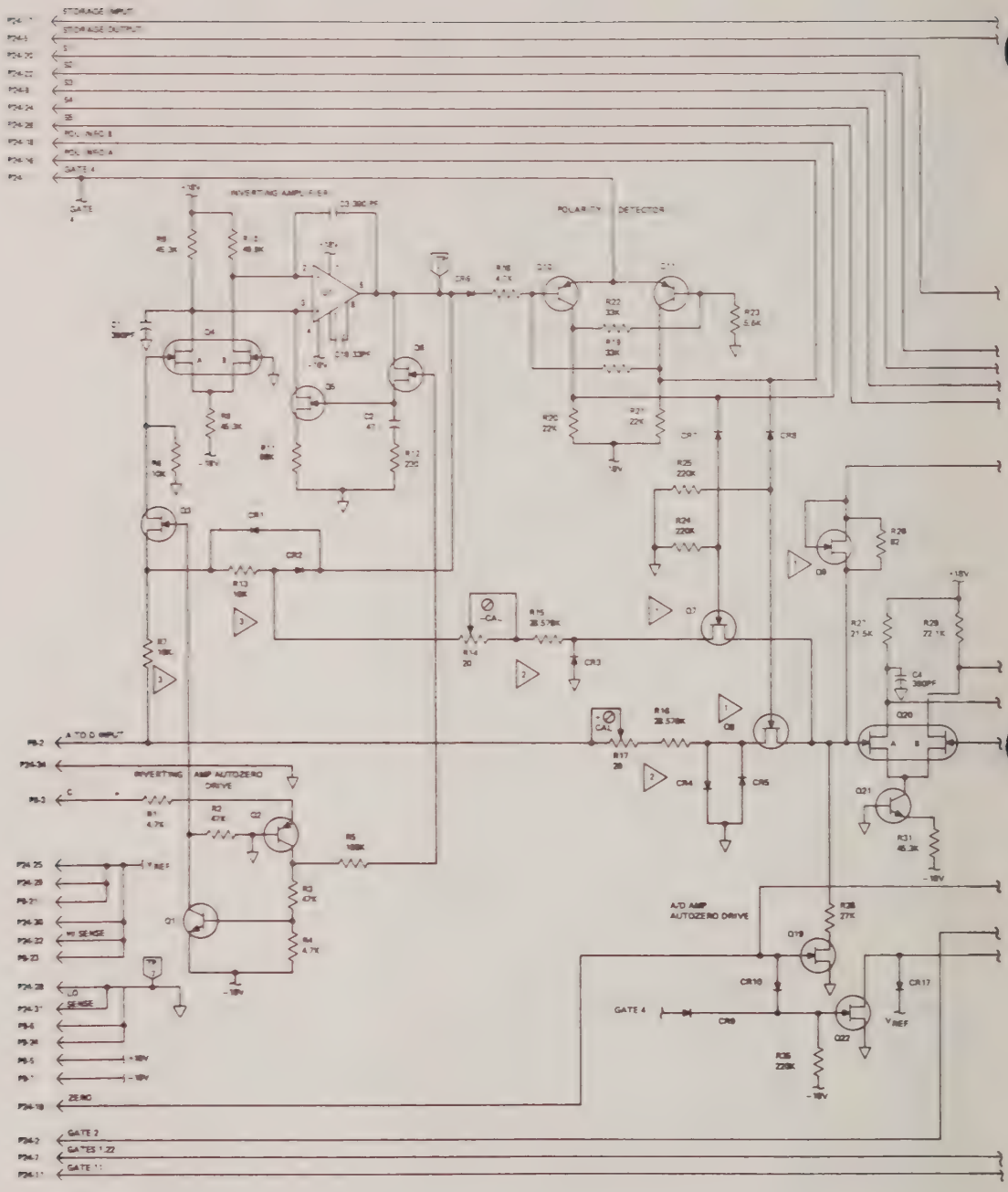
NOTES
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON
3. ▼ DENOTES LOGIC COMMON
4. 1 DENOTES MATCHED SET
5. ⊘ DENOTES INTERNAL ADJUSTMENT
6. 2 SEE WIRING DIAGRAM FOR CONNECTIONS TO P24.

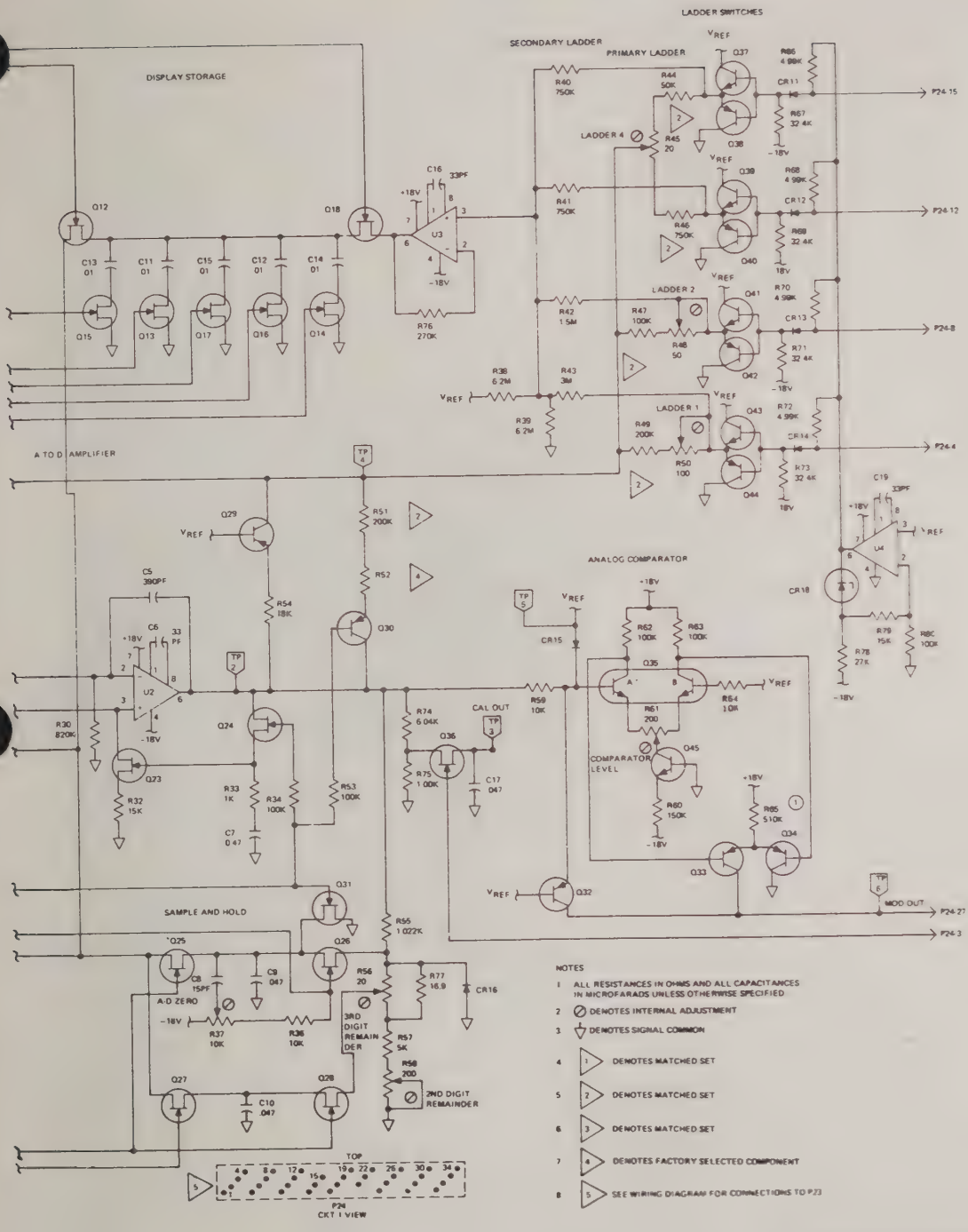
FUNCTIONAL SCHEMATIC DIAGRAM

A8
LOGIC

8400A—1004 | REV. b

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


STORAGE INPUT
STORAGE OUTPUT
S1
S2
S3
S4
S5
POL. INDIC. B
POL. INDIC. A
GATE 4
INVERTING AMPLIFIER
POLARITY DETECTOR
A TO D INPUT
INVERTING AMP AUTOZERO DRIVE
A/D AMP AUTOZERO DRIVE
Y REF
HI SENSE
LO SENSE
+18V
-18V
ZERO
GATE 2
GATES 1,22
GATE 11
CAL



NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED
2. ⊘ DENOTES INTERNAL ADJUSTMENT
3. ⏚ DENOTES SIGNAL COMMON
4. ▷1◁ DENOTES MATCHED SET
5. ▷2◁ DENOTES MATCHED SET
6. ▷3◁ DENOTES MATCHED SET
7. ▷4◁ DENOTES FACTORY SELECTED COMPONENT
8. ▷5◁ SEE WIRING DIAGRAM FOR CONNECTIONS TO P23

CHANGES

(1) R85 was 1M on SER. NO 123 thru approx. 287

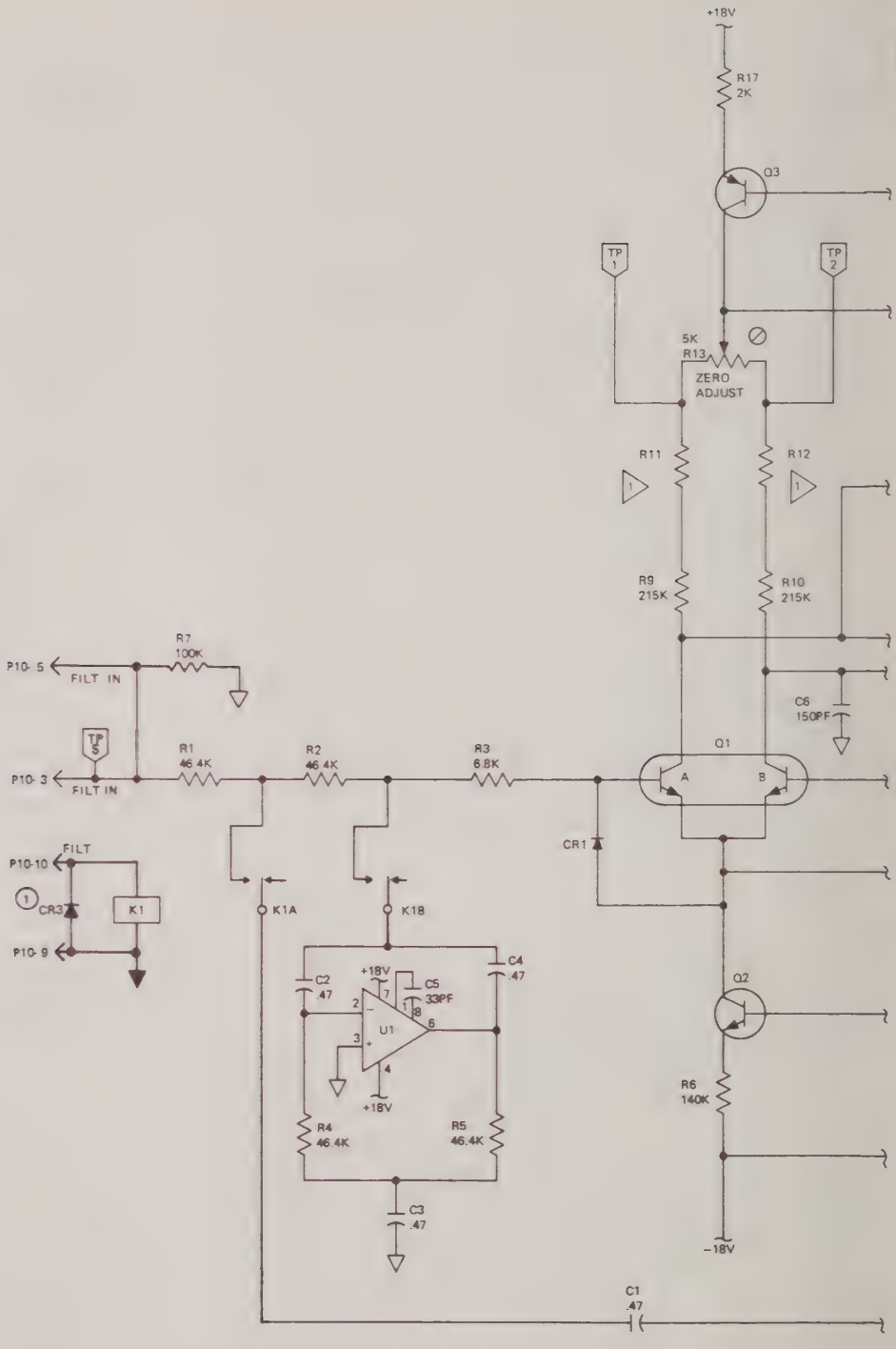
FUNCTIONAL SCHEMATIC DIAGRAM

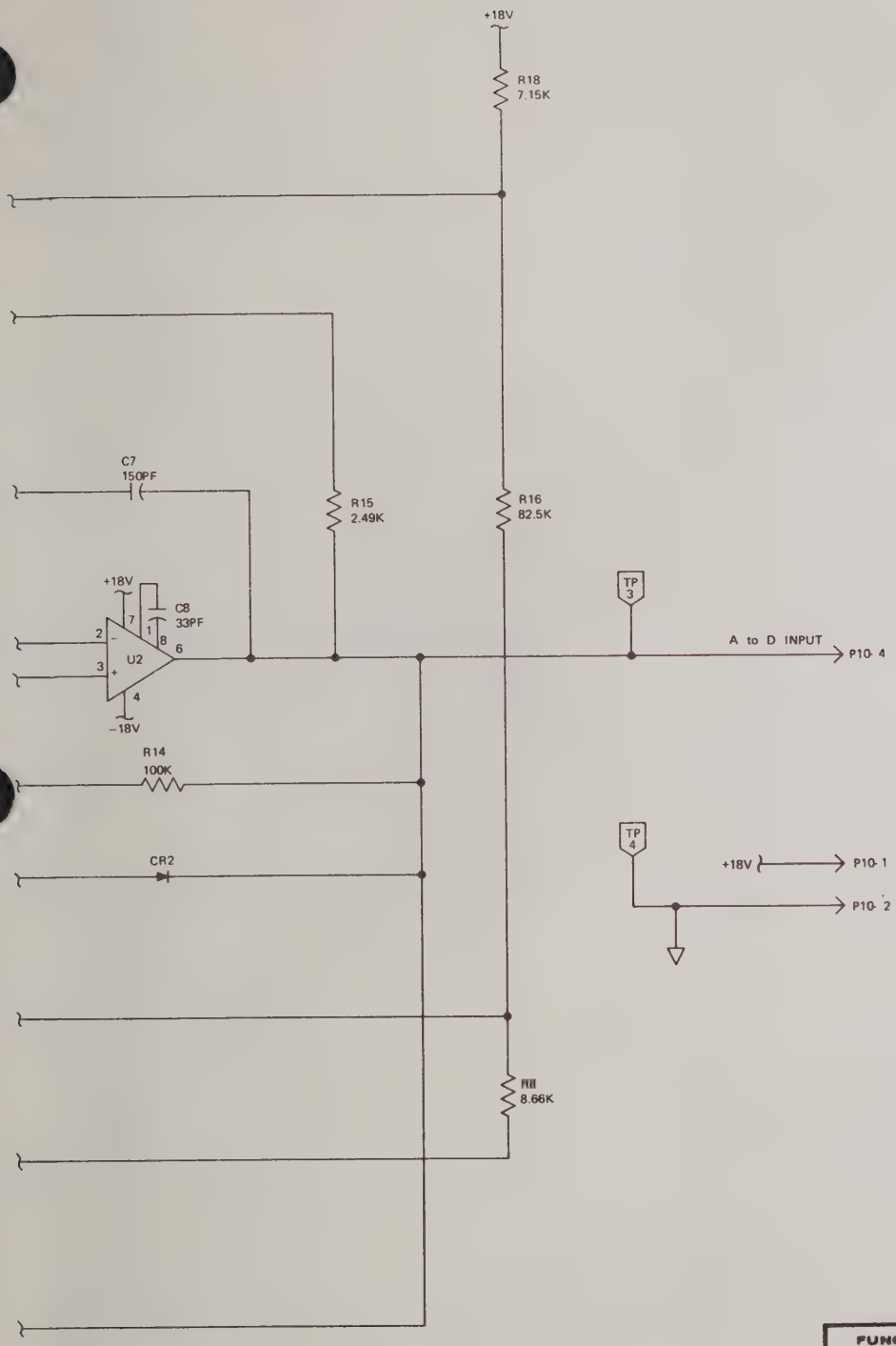
A9

A-TO-D CONVERTER

8400A–1003	REV b

JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


+18V
R17
2K
Q3
TP 1
TP 2
5K
R13
ZERO ADJUST
R11
R12
R9
215K
R10
215K
C6
150PF
Q1
A
B
R7
100K
P10-5
FILT IN
TP 5
P10-3
FILT IN
R1
46.4K
R2
46.4K
R3
6.8K
CR1
FILT
P10-10
CR3
K1
P10-9
K1A
K1B
C2
.47
+18V
C5
33PF
C4
.47
U1
Q2
R6
140K
R4
46.4K
R5
46.4K
C3
.47
-18V
C1
.47



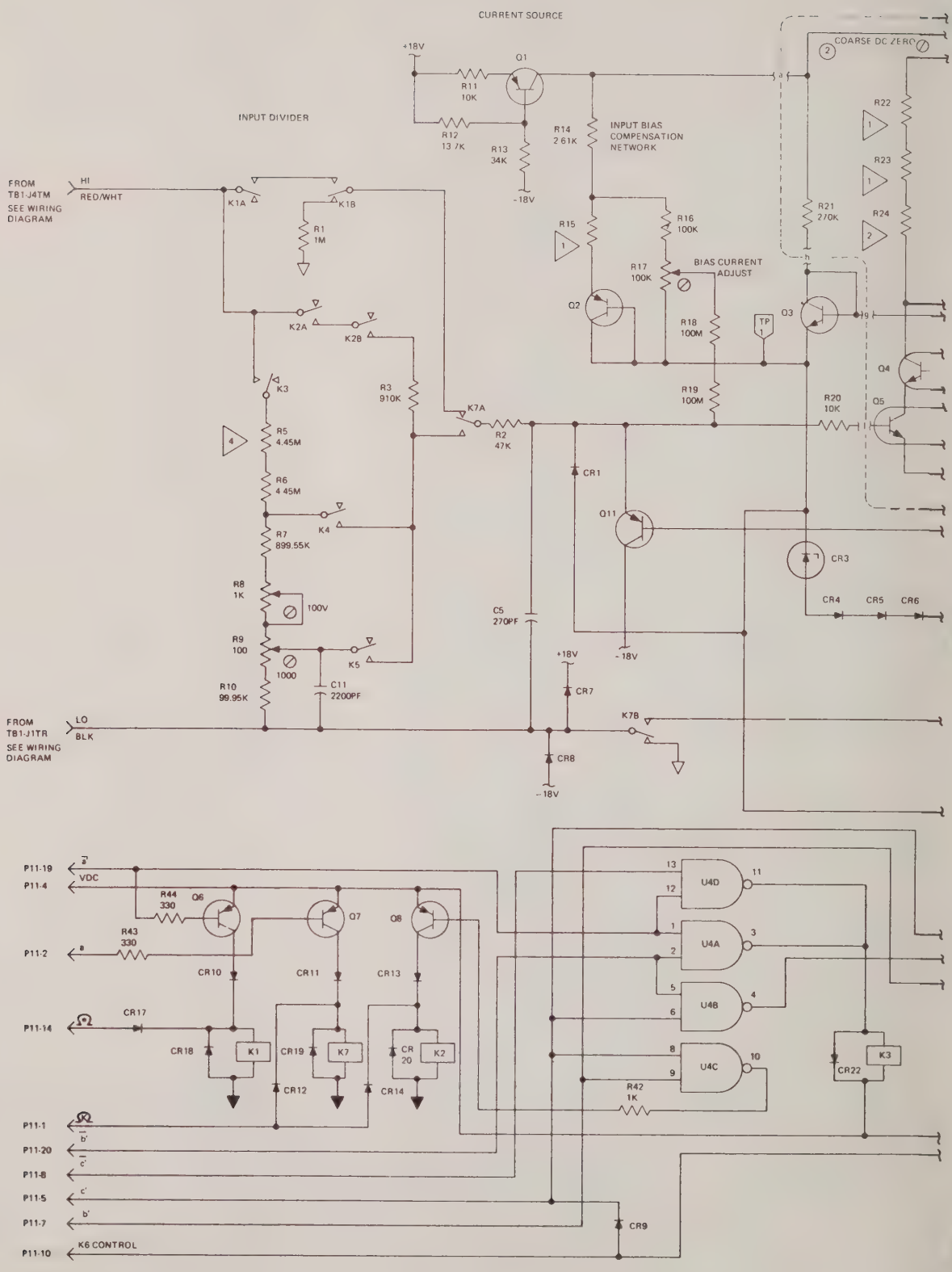
CHANGES

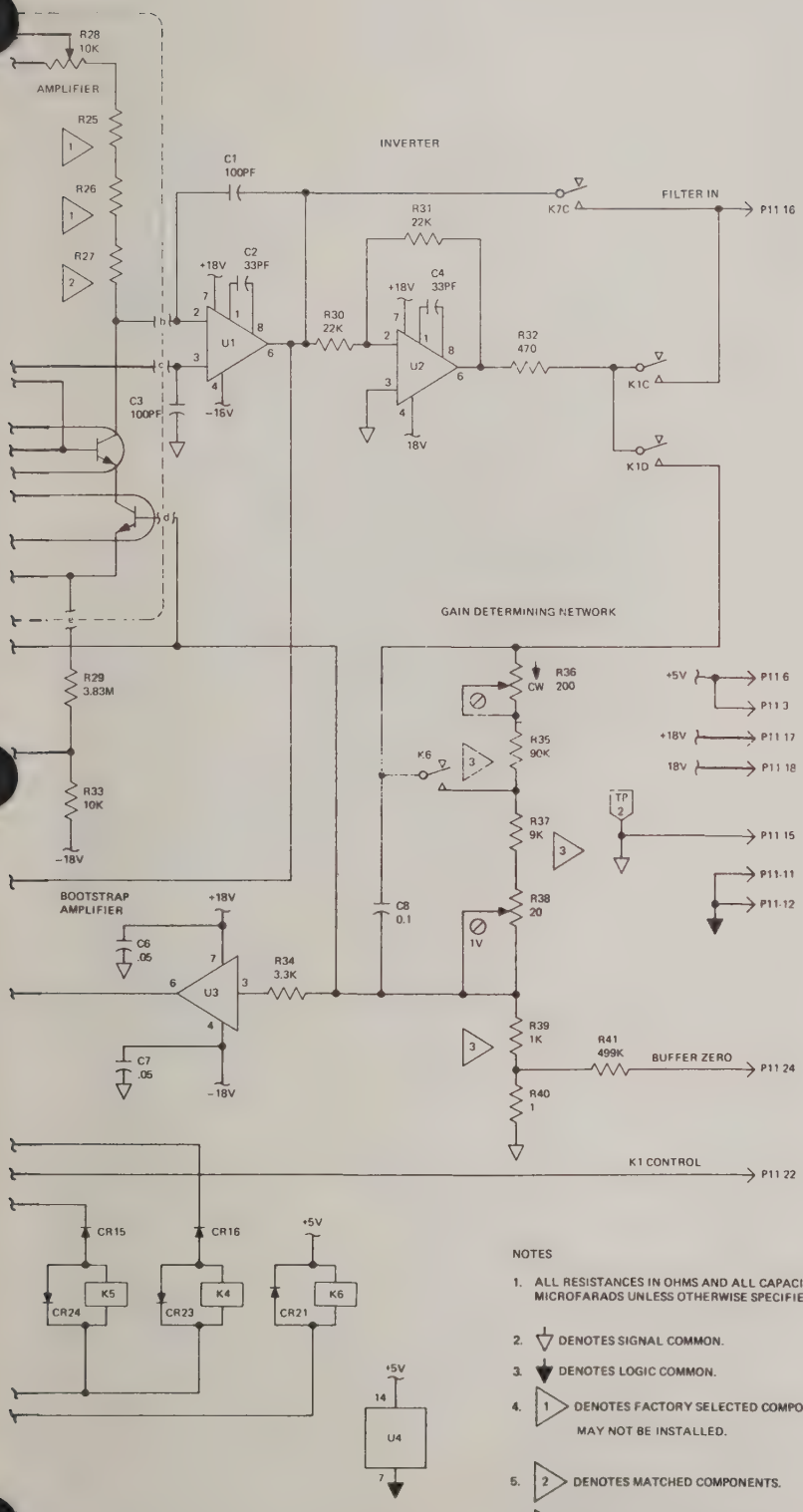
(1) CR3 ADDED AT SERIAL NO. 198 AND ABOVE

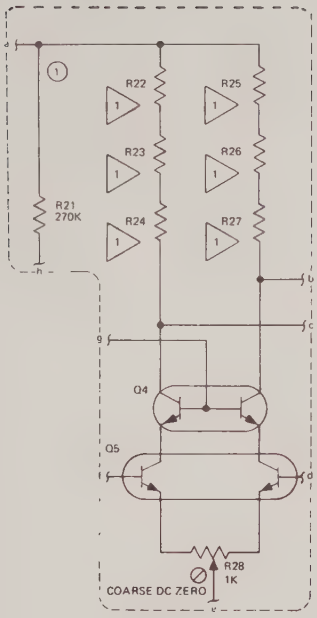
NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON.
3. ▼ DENOTES LOGIC COMMON.
4. (1)▷ FACTORY SELECTED
5. ⊘ DENOTES INTERNAL ADJUSTMENT

FUNCTIONAL SCHEMATIC DIAGRAM	
A10 ACTIVE FILTER	
8400A-1015	REV. b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	


CURRENT SOURCE
COARSE DC ZERO
INPUT DIVIDER
INPUT BIAS COMPENSATION NETWORK
BIAS CURRENT ADJUST
FROM TB1-J4TM SEE WIRING DIAGRAM
HI
RED/WHT
FROM TB1-J1TR SEE WIRING DIAGRAM
LO
BLK
+18V
-18V
100V
1000
P11-19
P11-4
VDC
P11-2
P11-14
P11-1
P11-20
P11-8
P11-5
P11-7
P11-10
K6 CONTROL





BUFFER RELAY LOGIC

	VOLTAGE RANGE				
	LO		HI		
RELAY	0.1	1.0	10	100	1000
K1	•	•			
K2			•		
K3				•	•
K4				•	
K5					•
K6		•			
K7			•	•	•

• INDICATES RELAY ENERGIZED

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▽ DENOTES SIGNAL COMMON.
3. ▼ DENOTES LOGIC COMMON.
4. (1) DENOTES FACTORY SELECTED COMPONENT. MAY NOT BE INSTALLED.
5. (2) DENOTES MATCHED COMPONENTS.
6. (3) R35, R37, and R39 ARE DIVIDER SET.
7. ⊘ DENOTES INTERNAL ADJUSTMENT.
8. (4) R5, R6, R7 and R10 ARE DIVIDER SET.

CHANGES

(1) SER. NO. 123 THRU 272

(2) SER. NO. 273 AND ABOVE

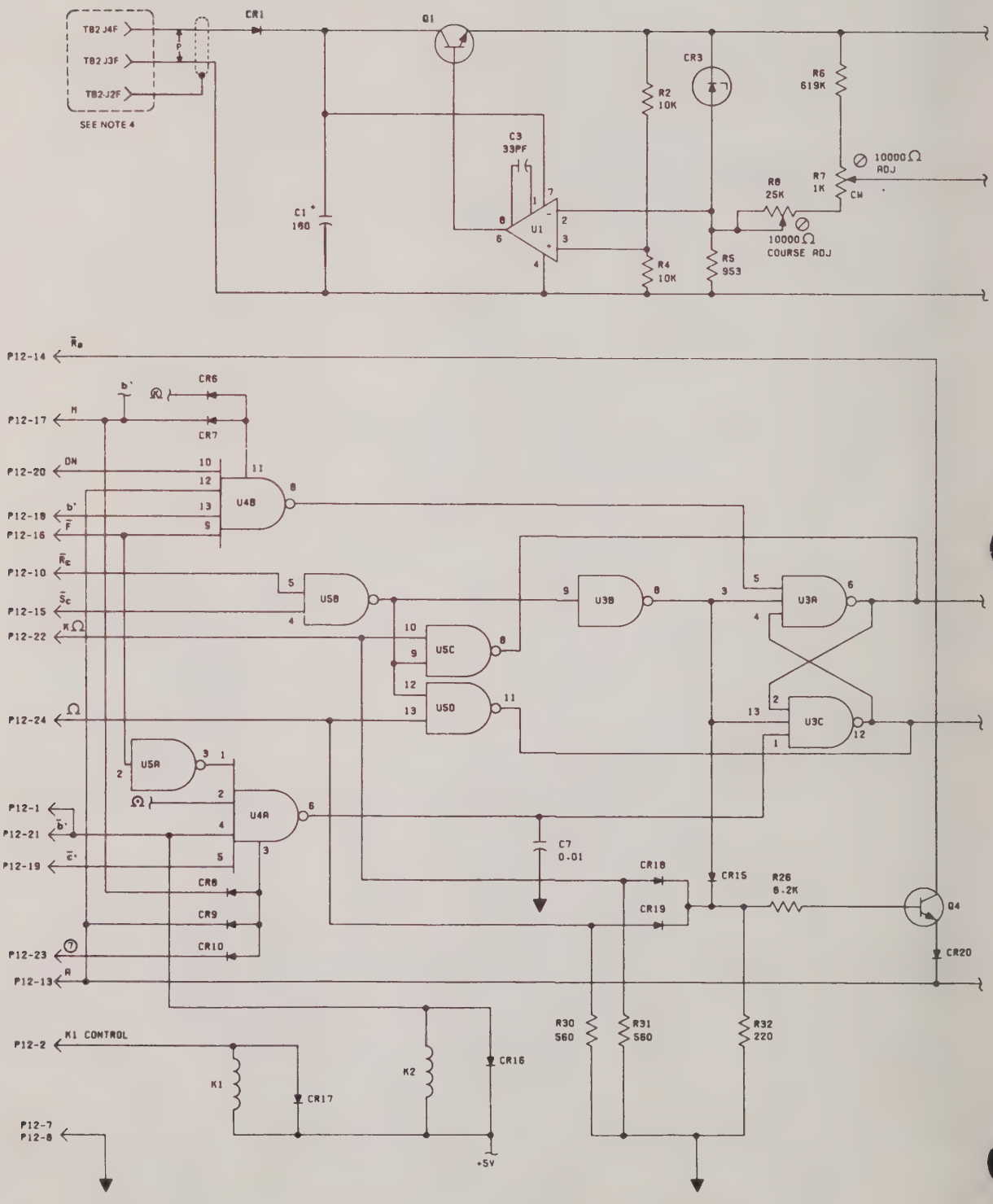
FUNCTIONAL SCHEMATIC DIAGRAM

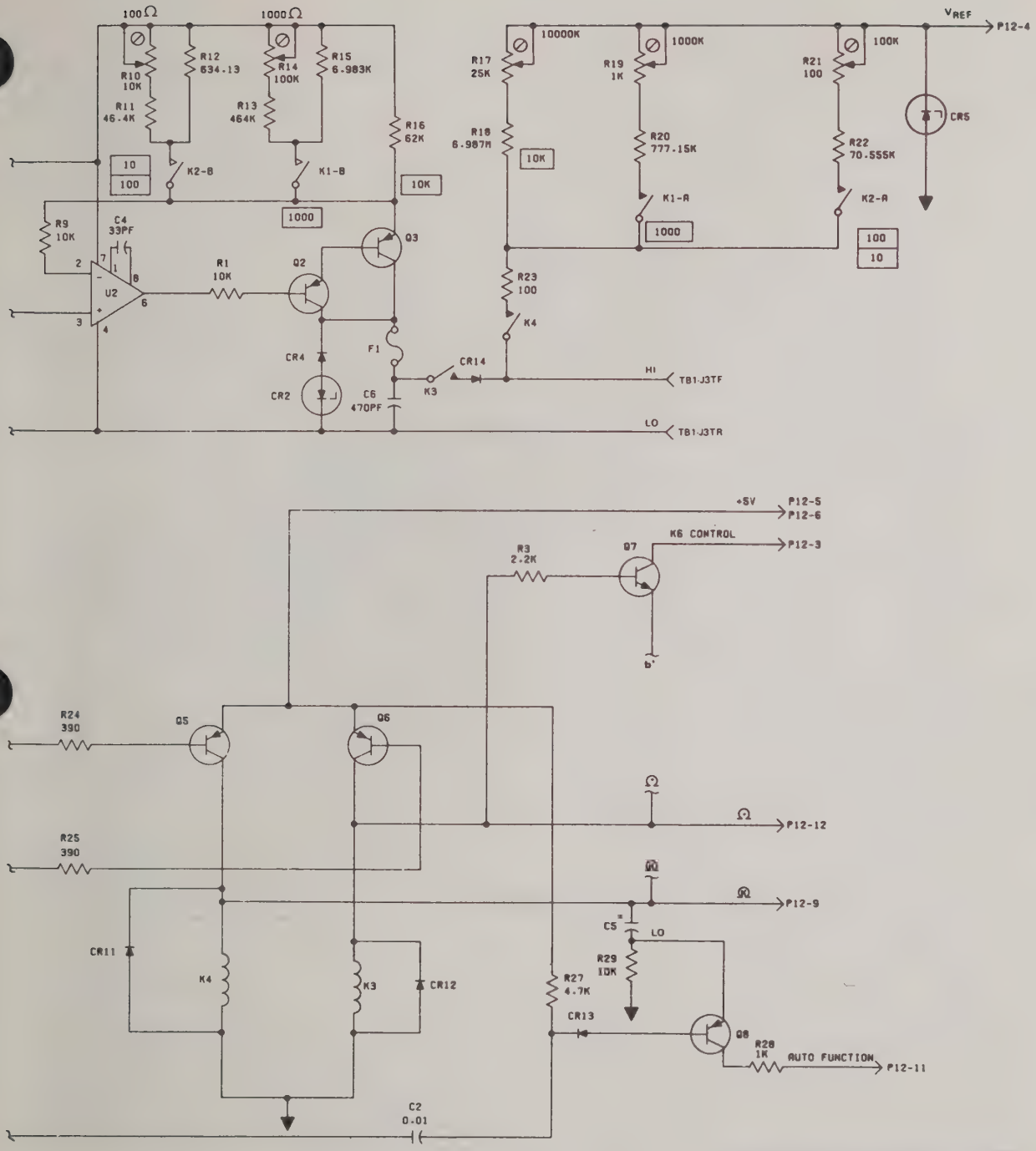
A11

BUFFER

8400A-1005 REV. b

FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133


TB2 J4F
TB2 J3F
TB2 J2F
SEE NOTE 4
CR1
Q1
R2 10K
CR3
R6 619K
C3 33PF
C1 100
U1
R4 10K
R5 953
R8 25K
10000Ω COURSE ADJ
R7 1K CW
10000Ω ADJ
P12-14
P12-17
P12-20
P12-18
P12-16
P12-10
P12-15
P12-22
P12-24
P12-1
P12-21
P12-19
P12-23
P12-13
P12-2
P12-7
P12-8
CR6
CR7
U4B
U5B
U5C
U5D
U3B
U3A
U3C
U5A
U4A
C7 0.01
CR8
CR9
CR10
CR18
CR19
CR15
R26 6.2K
Q4
CR20
R30 560
R31 560
R32 220
K1 CONTROL
K1
K2
CR16
CR17
+5V

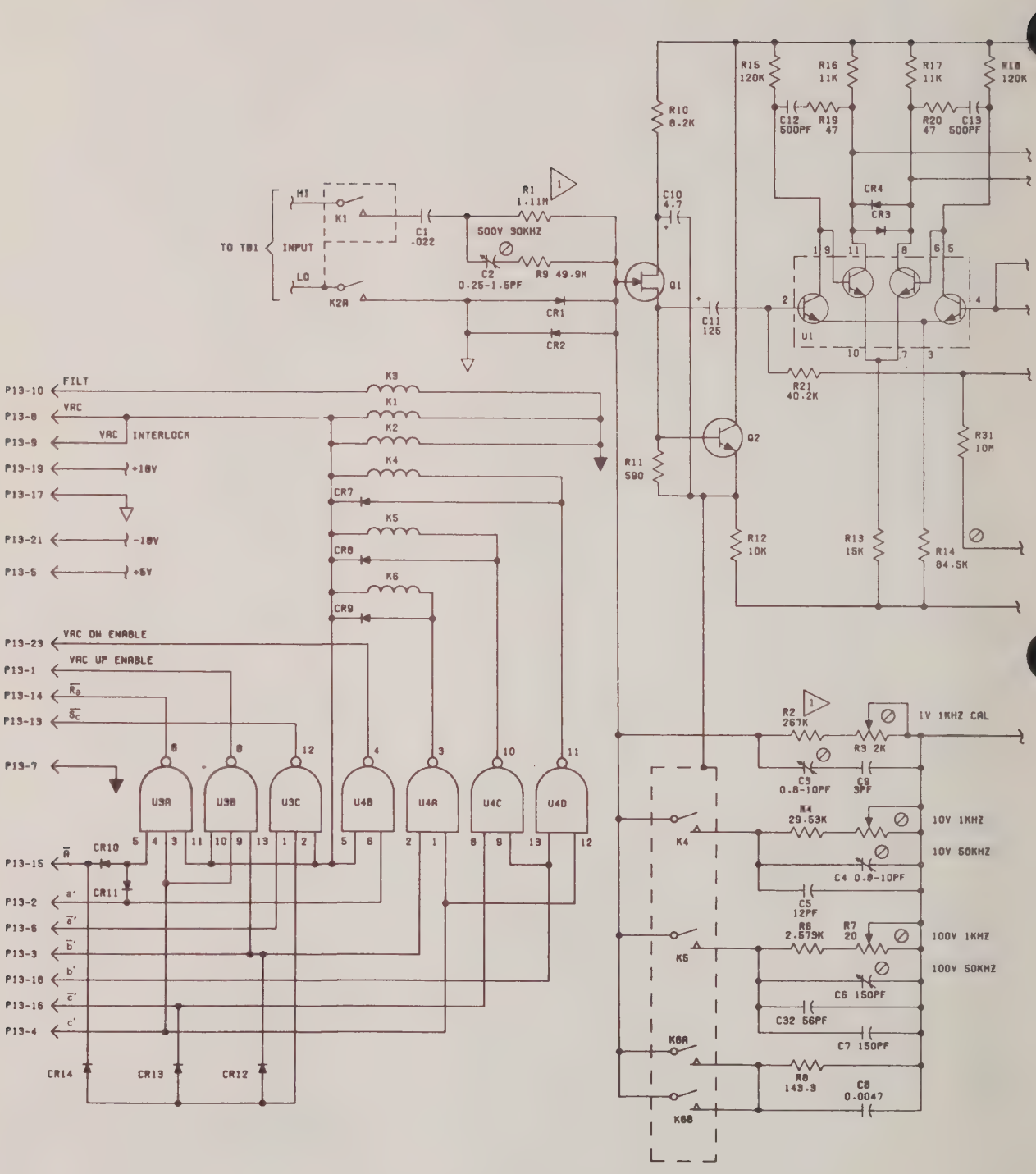


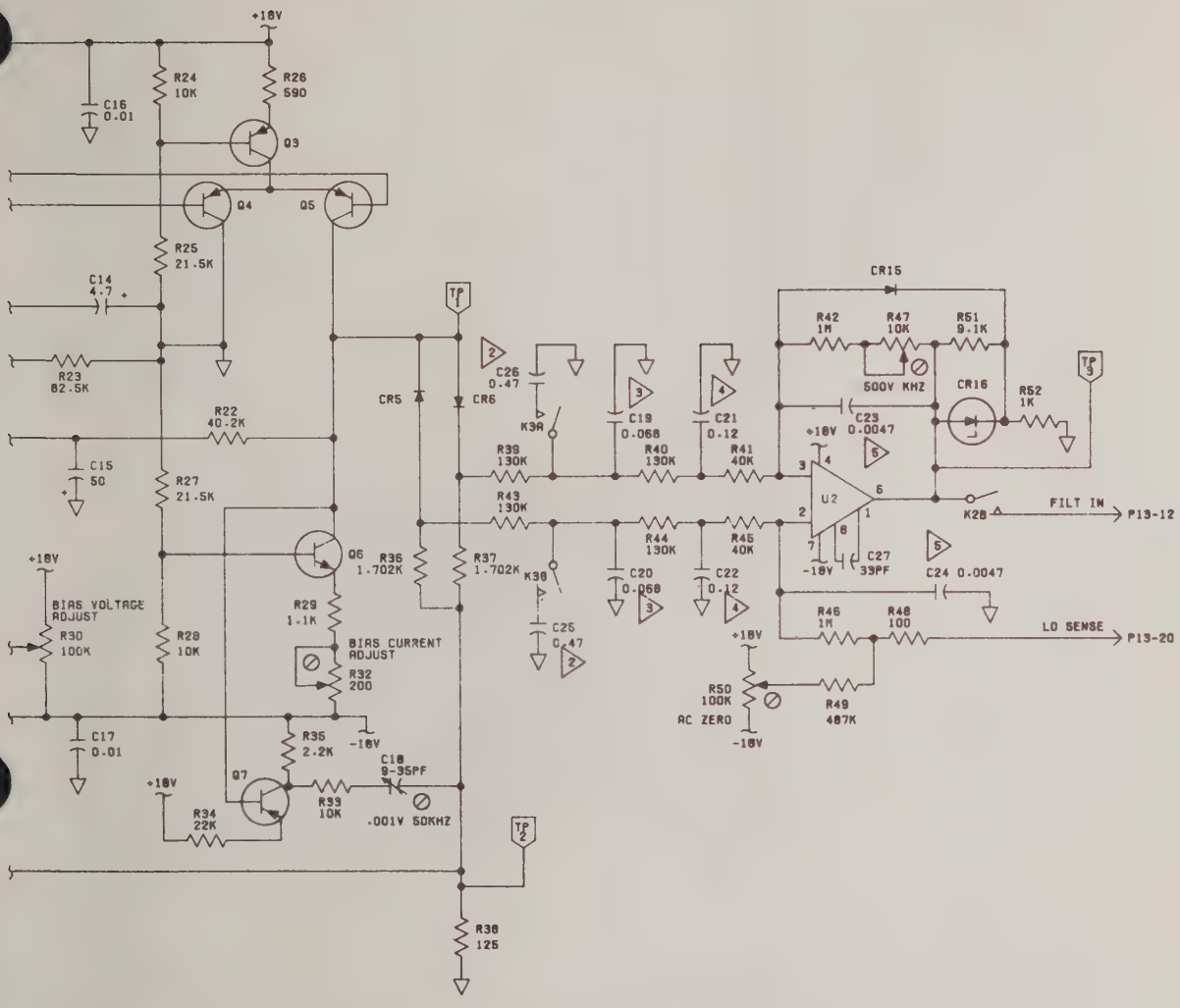
IC	PIN CONNECTIONS	
	+5VDC	COMMON
U3	14	7
U4	14	7
U5	14	7

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON
3. ⊘ DENOTES INTERNAL ADJUSTMENT
4. SEE WIRING DIAGRAM

FUNCTIONAL SCHEMATIC DIAGRAM	
A12 OHMS CONVERTER	
8400A–1010	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	


TO TB1
INPUT
HI
LO
K1
K2A
C1 .022
R1 1.11M
500V 30KHZ
C2 0.25-1.5PF
R9 49.9K
CR1
CR2
C10 4.7
Q1
C11 125
R10 8.2K
R15 120K
R16 11K
R17 11K
R18 120K
C12 500PF
R19 47
R20 47
C13 500PF
CR4
CR3
U1
R21 40.2K
Q2
R11 590
R12 10K
R13 15K
R14 84.5K
R31 10M
P13-10 FILT
P13-8 VAC
P13-9 VAC INTERLOCK
P13-19 +18V
P13-17
P13-21 -18V
P13-5 +5V
K3
K1
K2
K4
CR7
K5
CR8
K6
CR9
P13-23 VAC DN ENABLE
P13-1 VAC UP ENABLE
P13-14 $\overline{R_a}$
P13-13 $\overline{S_c}$
P13-7
U3A
U3B
U3C
U4B
U4A
U4C
U4D
P13-15 $\overline{R}$
CR10
CR11
P13-2 a'
P13-8 $\overline{a'}$
P13-3 $\overline{b'}$
P13-18 b'
P13-16 $\overline{c'}$
P13-4 c'
CR14
CR13
CR12
R2 267K
R3 2K
1V 1KHZ CAL
C3 0.8-10PF
C9 3PF
K4
R4 29.53K
10V 1KHZ
10V 50KHZ
C4 0.8-10PF
C5 12PF
K5
R6 2.579K
R7 20
100V 1KHZ
100V 50KHZ
C6 150PF
C32 56PF
C7 150PF
K6A
K6B
R8 143.3
C8 0.0047



IC	PIN CONNECTIONS	
	+5V	COMMON
U3	14	7
U4	14	7

NOTES

1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ⏚ DENOTES SIGNAL COMMON
3. ▼ DENOTES LOGIC COMMON
4. ⊘ DENOTES INTERNAL ADJUSTMENT
5. (1) THRU (5) DENOTES MATCHED SET.
6. - - - - - - - GUARD SHIELD

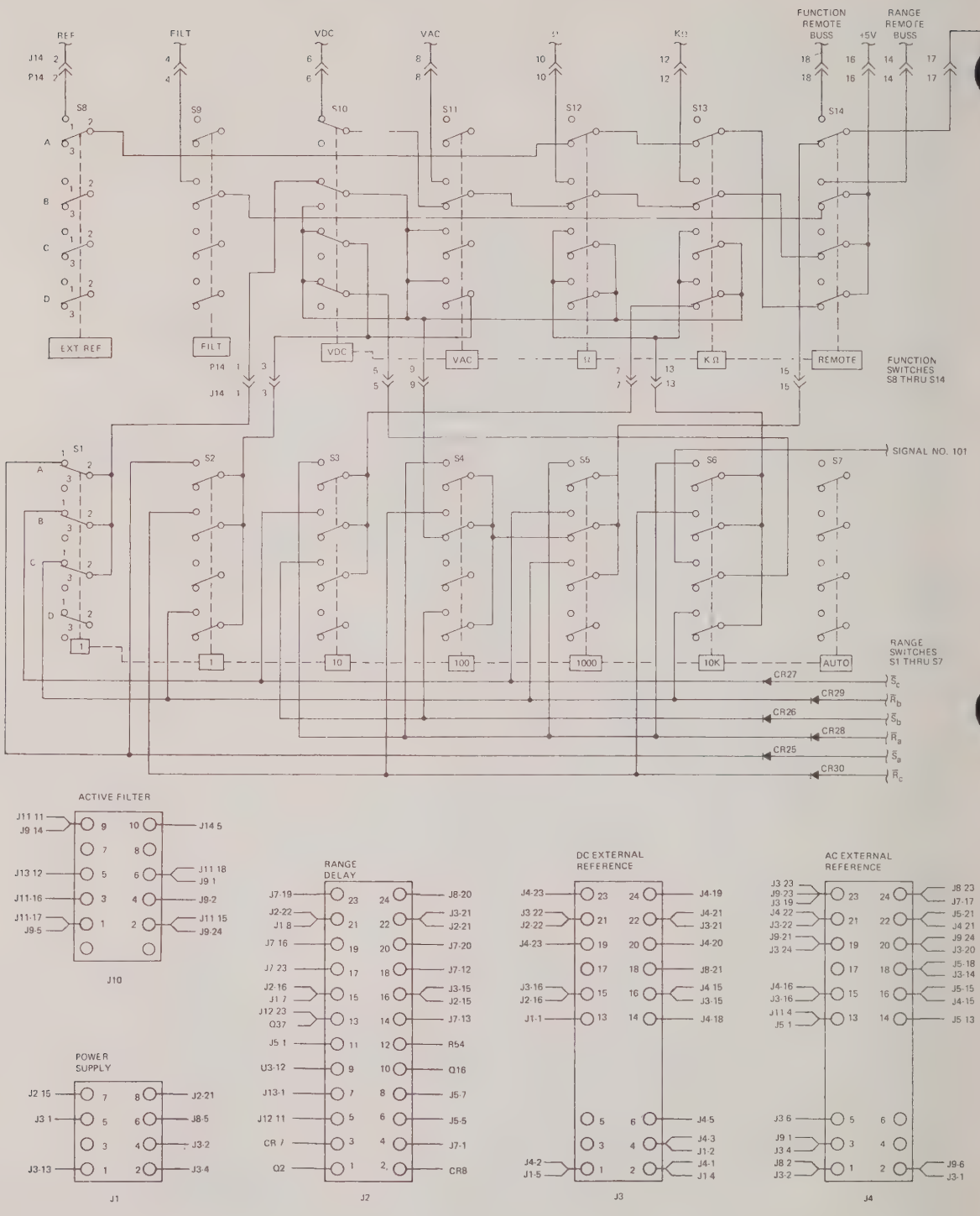
FUNCTIONAL SCHEMATIC DIAGRAM

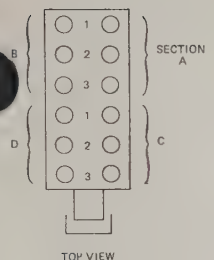
A13

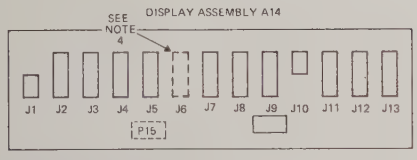
AC CONVERTER

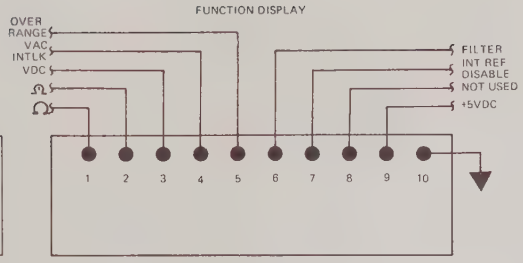
8400A-1007 REV b

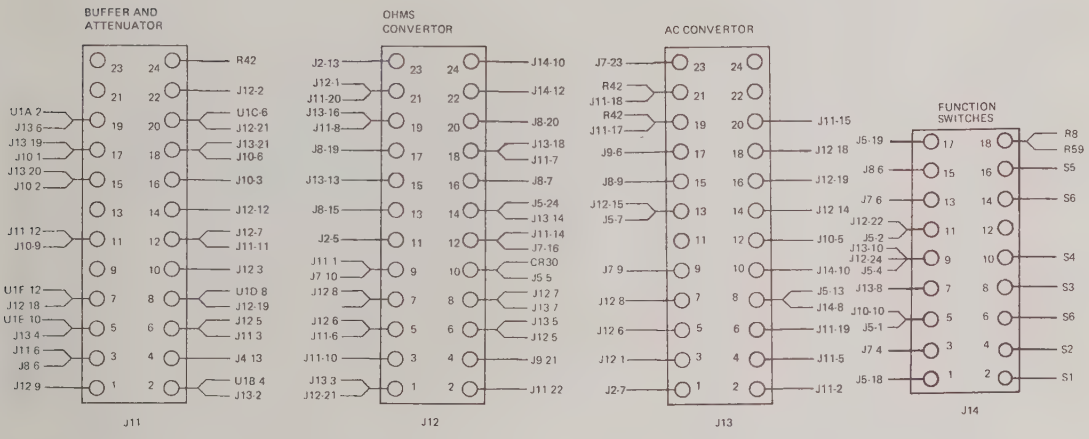
FLUKE JOHN FLUKE MFG. CO., INC.
P.O. Box 7428 Seattle, Washington 98133

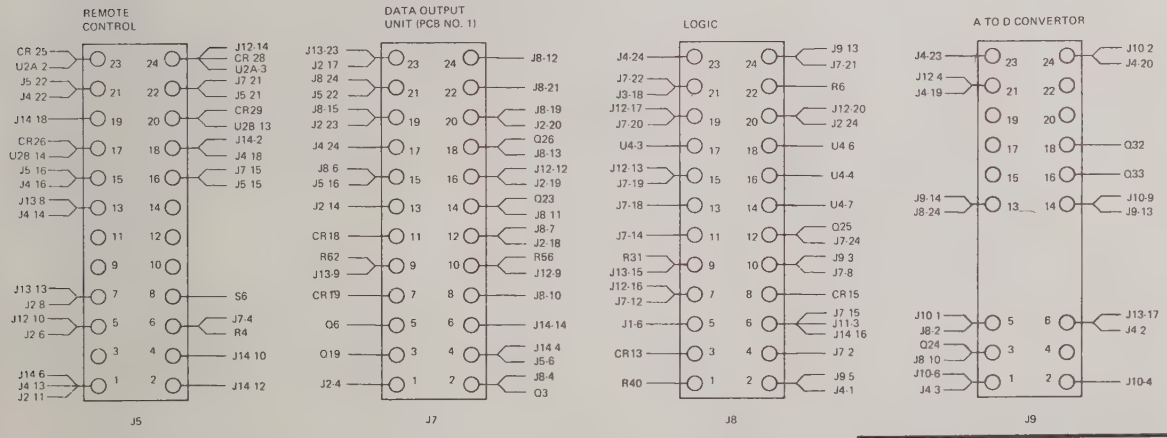

REF
FILT
VDC
VAC
Ω
KΩ
FUNCTION REMOTE BUSS
+5V
RANGE REMOTE BUSS
S8
S9
S10
S11
S12
S13
S14
EXT REF
FILT
VDC
VAC
Ω
KΩ
REMOTE
FUNCTION SWITCHES S8 THRU S14
S1
S2
S3
S4
S5
S6
S7
SIGNAL NO. 101
1
10
100
1000
10K
AUTO
RANGE SWITCHES S1 THRU S7
CR27
CR29
CR26
CR28
CR25
CR30
ACTIVE FILTER
J10
POWER SUPPLY
J1
RANGE DELAY
J2
DC EXTERNAL REFERENCE
J3
AC EXTERNAL REFERENCE
J4




DISPLAY ASSEMBLY A14
SEE NOTE 4
J1 J2 J3 J4 J5 J6 J7 J8 J9 J10 J11 J12 J13
P15
CONNECTOR LOCATION - VIEWED FROM TOP FRONT OF INSTRUMENT



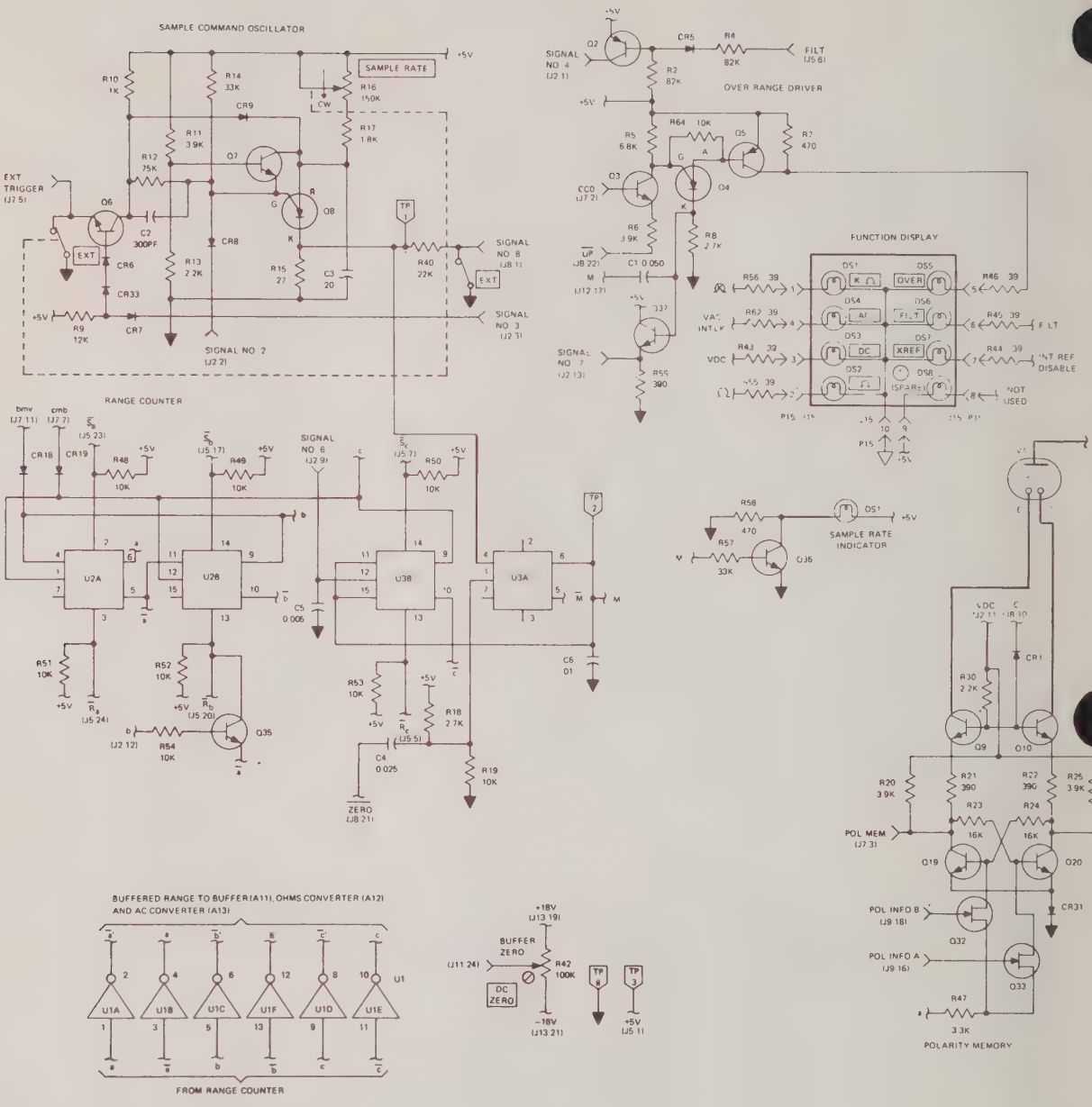


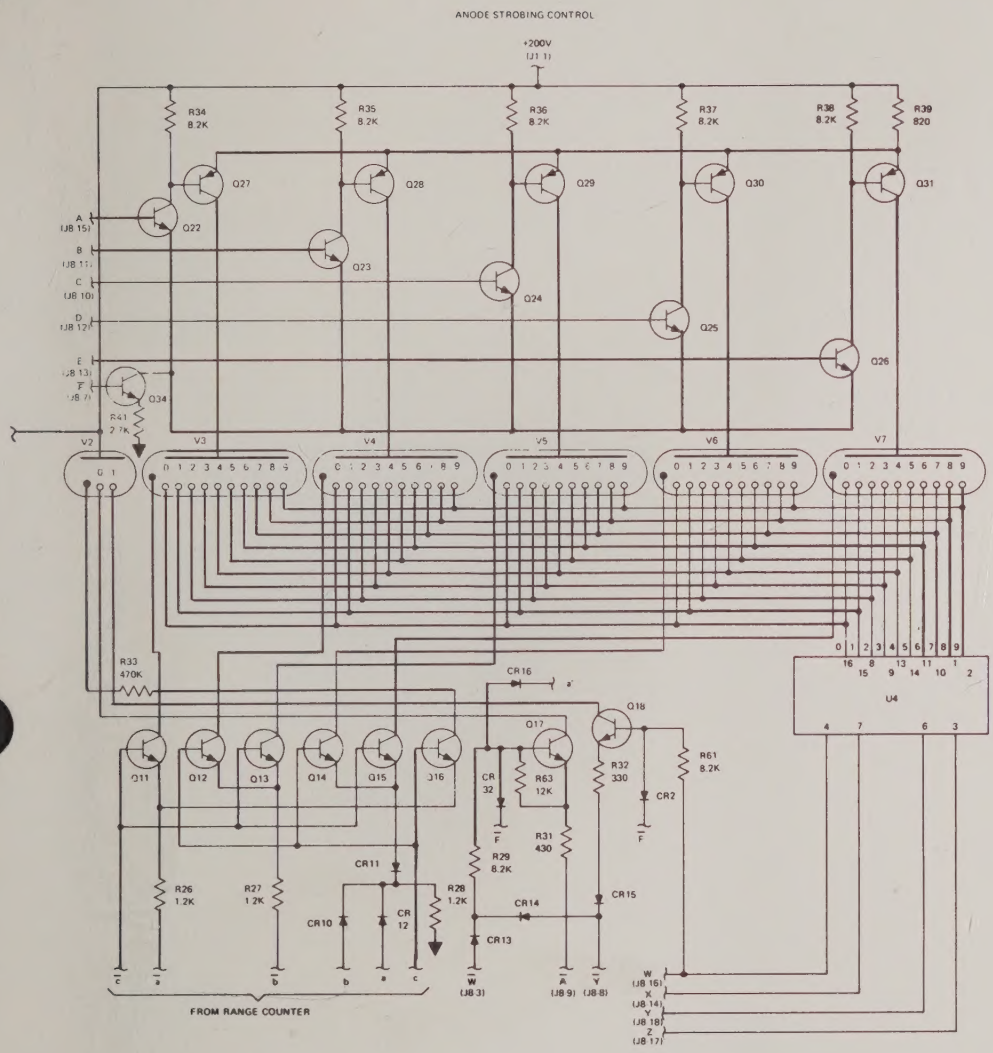


NOTES:

1. ▼ DENOTES LOGIC COMMON.
2. ▭ DENOTES FRONT PANEL LOCATION
3. CONNECTORS J6, J22, J23, AND J24 MATE WITH P6, P22, P23, AND P24, RESPECTIVELY IN HARD -WIRED, NON-SEPARABLE CONFIGURATION. SEE ASS'Y INTERCONNECT DIAGRAM.

FUNCTIONAL SCHEMATIC DIAGRAM	
A14 DISPLAY SHEET 1 of 2	
8400A-1002	REV b
FLUKE JOHN FLUKE MFG. CO., INC. P O Box 7428 Seattle, Washington 98133	


SAMPLE COMMAND OSCILLATOR
SAMPLE RATE
EXT TRIGGER (J7 5)
SIGNAL NO 8 (J8 1)
SIGNAL NO 3 (J2 5)
SIGNAL NO 2 (J2 2)
OVER RANGE DRIVER
SIGNAL NO 4 (J2 1)
FILT (J5 6)
FUNCTION DISPLAY
OVER
FLT
DC
XREF
INT REF DISABLE
NOT USED
SAMPLE RATE INDICATOR
RANGE COUNTER
SIGNAL NO 6 (J2 9)
ZERO (J8 21)
POLARITY MEMORY
POL MEM (J7 3)
POL INFO B (J9 18)
POL INFO A (J9 16)
BUFFERED RANGE TO BUFFER (A11), OHMS CONVERTER (A12) AND AC CONVERTER (A13)
FROM RANGE COUNTER
BUFFER ZERO
DC ZERO
+18V (J13 19)
−18V (J13 21)
+5V (J5 11)



IC	PIN CONNECTIONS	
	+5V	COMMON
U1	14	7
U2	16	8
U3	16	8
U4	5	12

NOTES

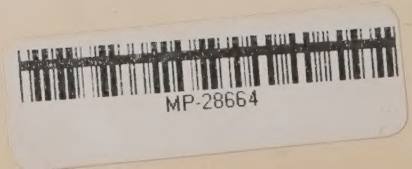
1. ALL RESISTANCES IN OHMS AND ALL CAPACITANCES IN MICROFARADS UNLESS OTHERWISE SPECIFIED.
2. ▼ DENOTES LOGIC COMMON.
3. ▭ DENOTES FRONT PANEL LOCATION.

CHANGES:

(1) DS8 DELETED AT SERIAL NO. 209 AND ABOVE.

FUNCTIONAL SCHEMATIC DIAGRAM	
A14 DISPLAY SHEET 2 of 2	
8400A-1002	REV. b
FLUKE JOHN FLUKE MFG. CO., INC. P.O. Box 7428 Seattle, Washington 98133	

NOTES


MP-28664